Static Program Analysis: Caches in WCET Analysis

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Outline

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1. Caches
2. Cache Analysis for Least-Recently-Used
3. Beyond Least-Recently-Used
   - Predictability Metrics
   - Relative Competitiveness
   - Sensitivity – Caches and Measurement-Based Timing Analysis
4. Summary

Outline

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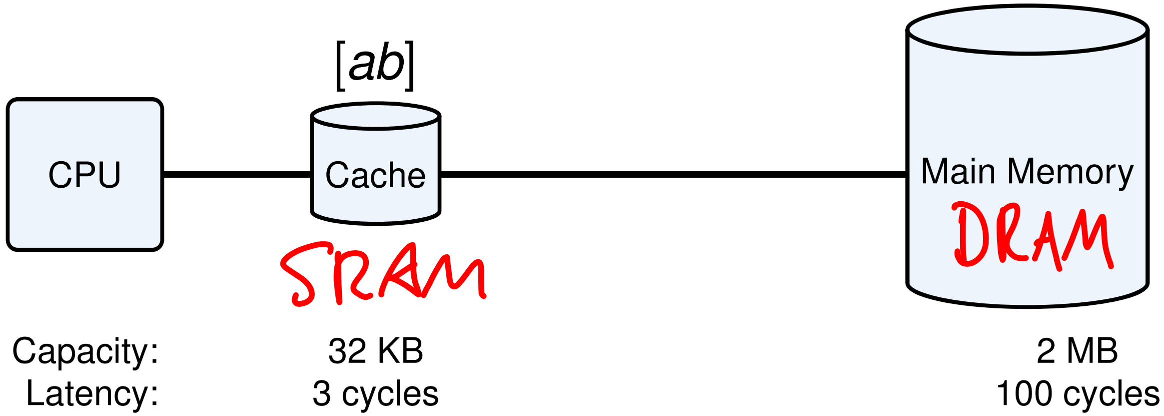
Caches

- How they work:
  - dynamically
  - managed by replacement policy



- Why they work: *principle of locality*
  - spatial
  - temporal

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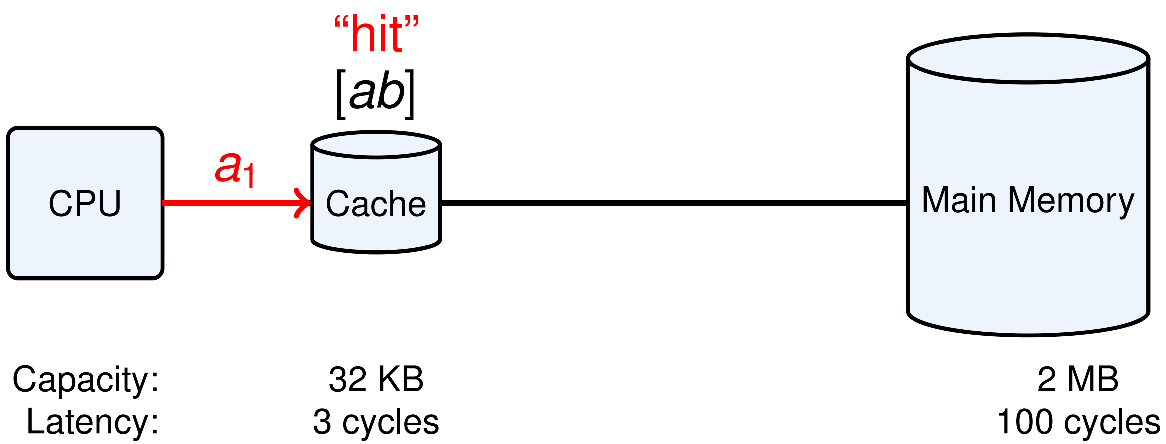

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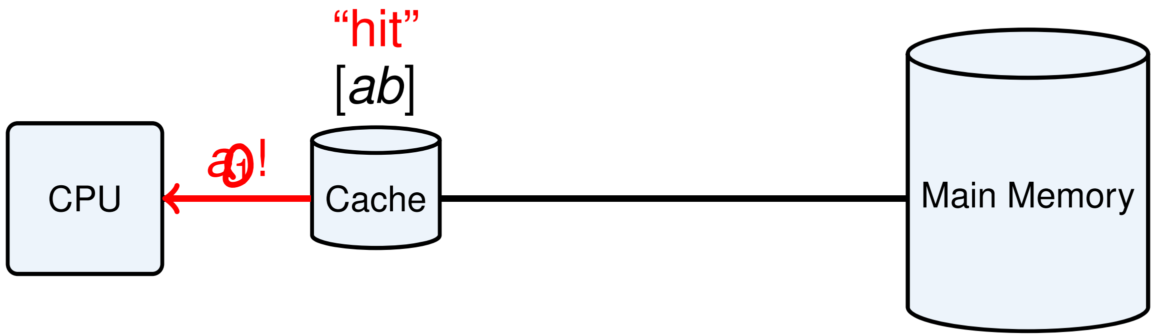

Capacity:	32 KB	2 MB
Latency:	3 cycles	100 cycles

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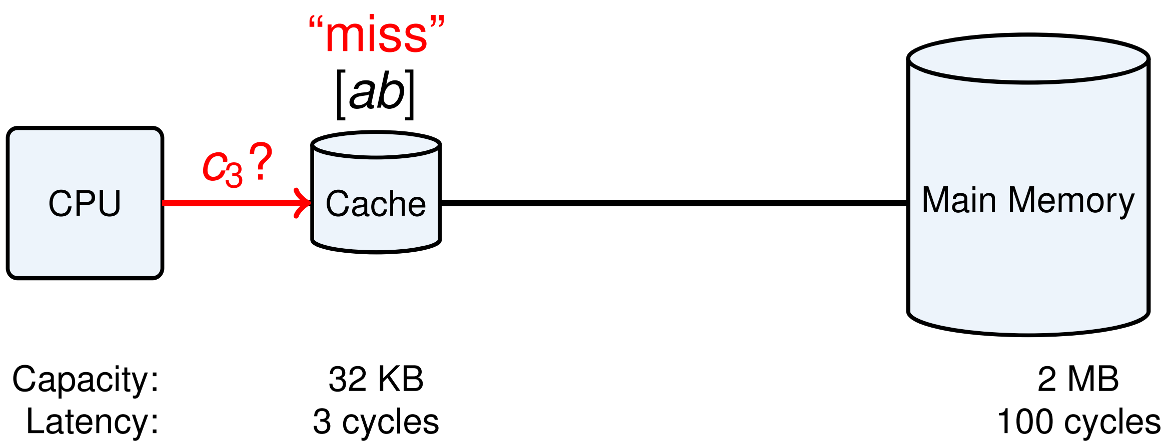

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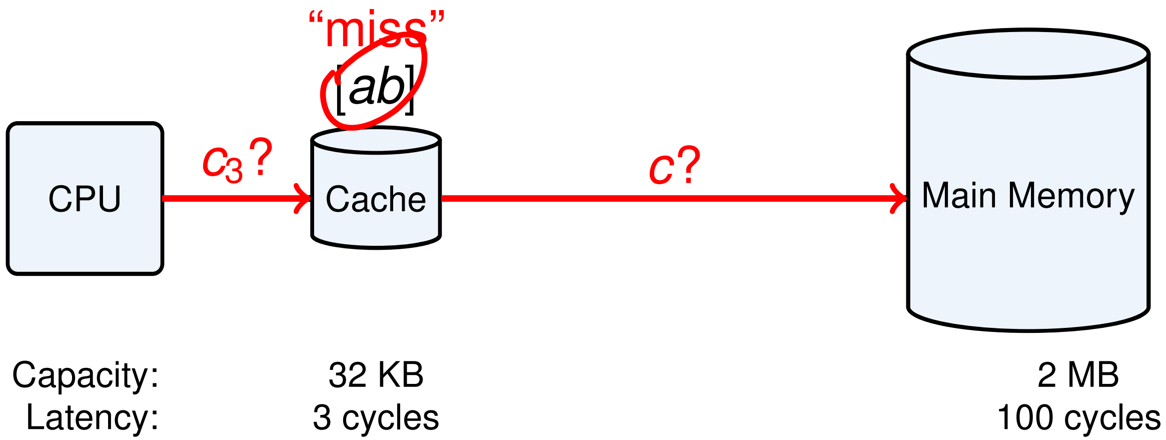

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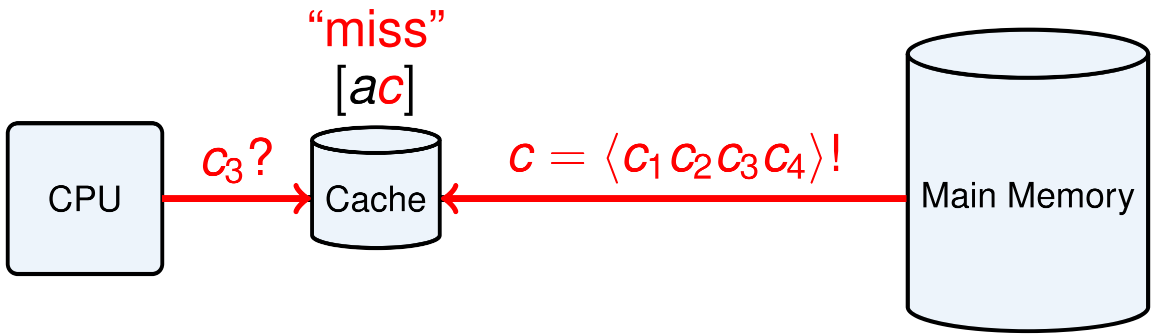

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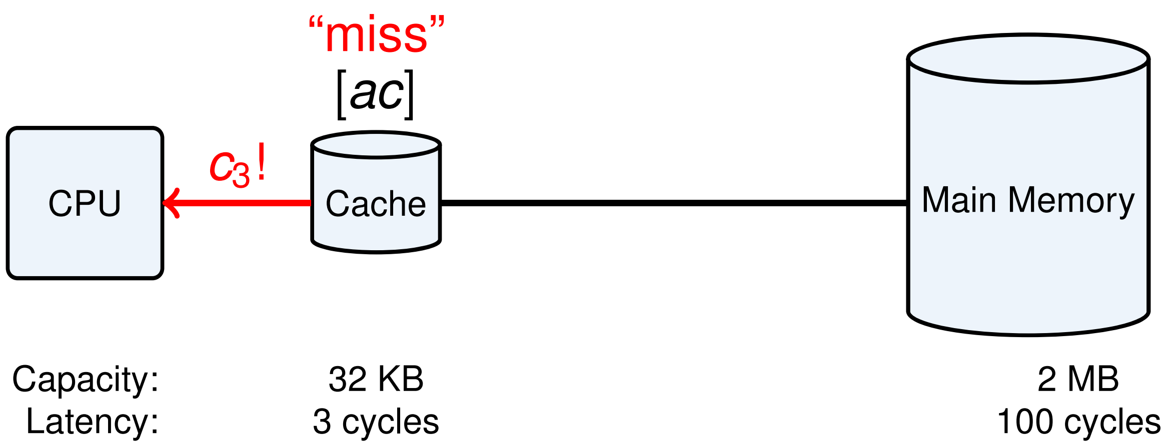

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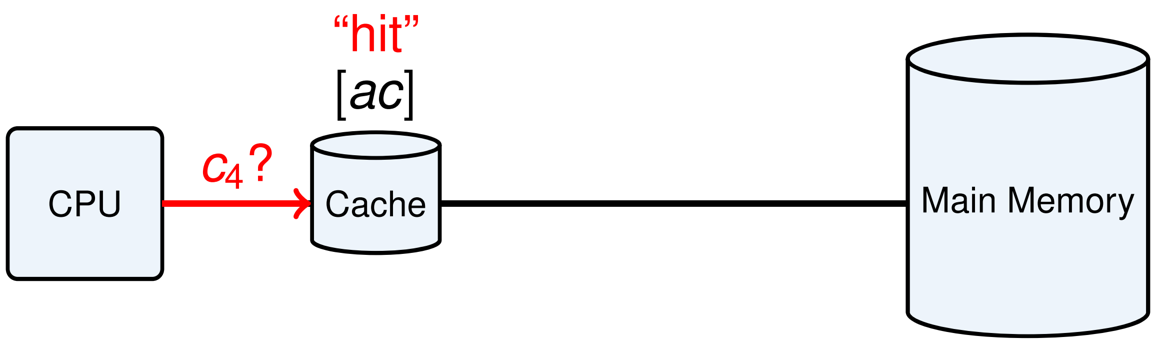

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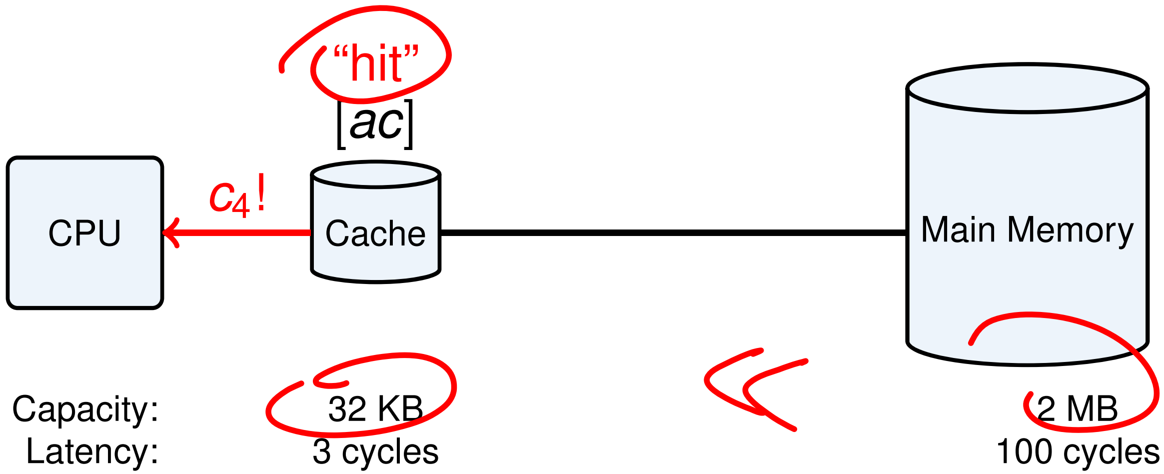

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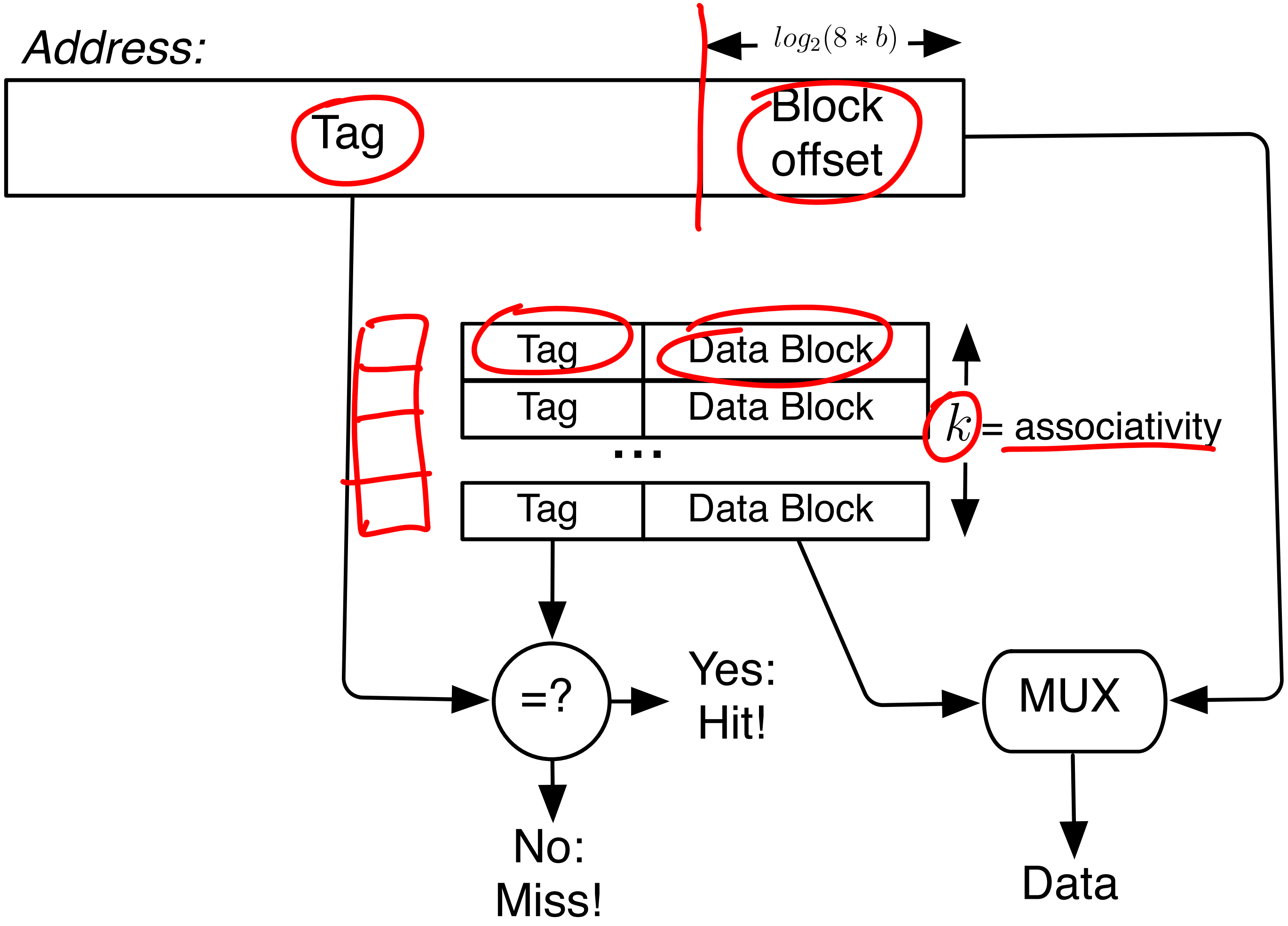
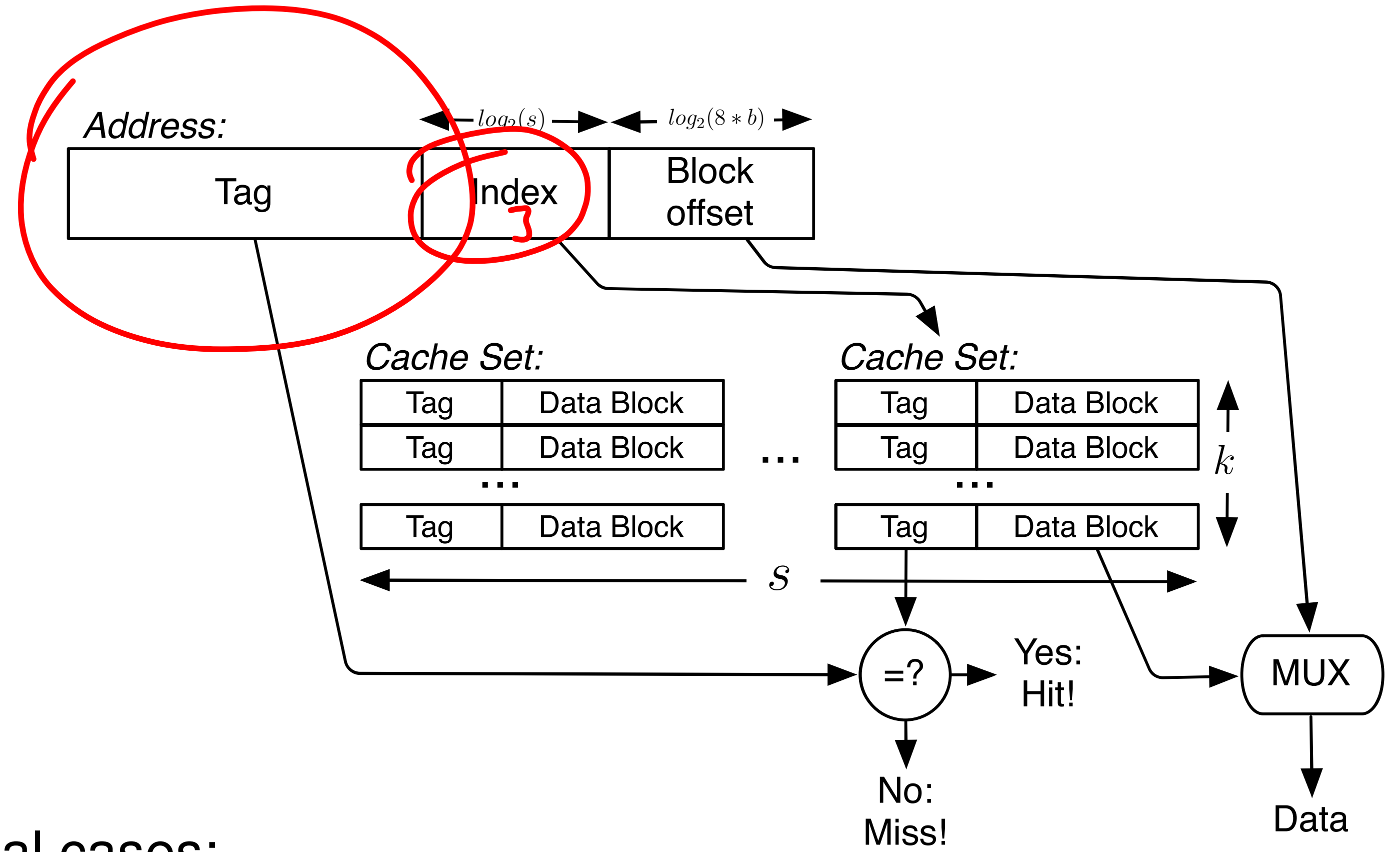
Fully-Associative Caches



Set-Associative Caches



Special cases:

- direct-mapped cache: only one line per cache set
- fully-associative cache: only one cache set

Cache Replacement Policies

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- Least-Recently-Used (LRU) used in
  INTEL PENTIUM I and MIPS 24K/34K
- First-In First-Out (FIFO or Round-Robin) used in
  MOTOROLA POWERPC 56X, INTEL XSCALE, ARM9, ARM11
- Pseudo-LRU (PLRU) used in
  INTEL PENTIUM II-IV and POWERPC 75X
- Most Recently Used (MRU) as described in literature
  INTEL NEHALEM

Each cache set is treated independently:
$\longrightarrow$ Set-associative caches are compositions of fully-associative caches.

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Cache Analysis

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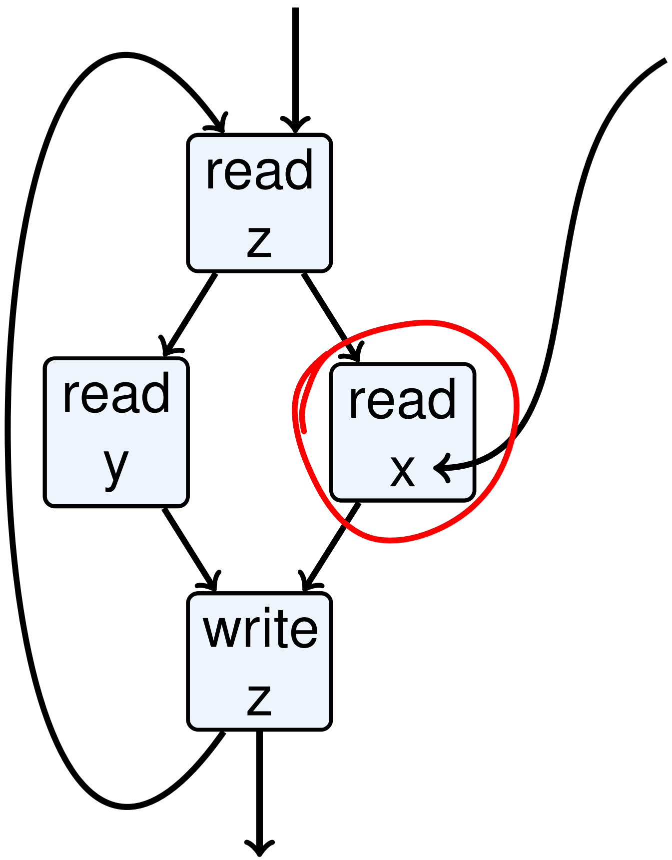
Two types of cache analyses:

1. Local guarantees: classification of individual accesses
   - May-Analysis $\longrightarrow$ Overapproximates cache contents
   - Must-Analysis $\longrightarrow$ Underapproximates cache contents
2. Global guarantees: bounds on cache hits/misses

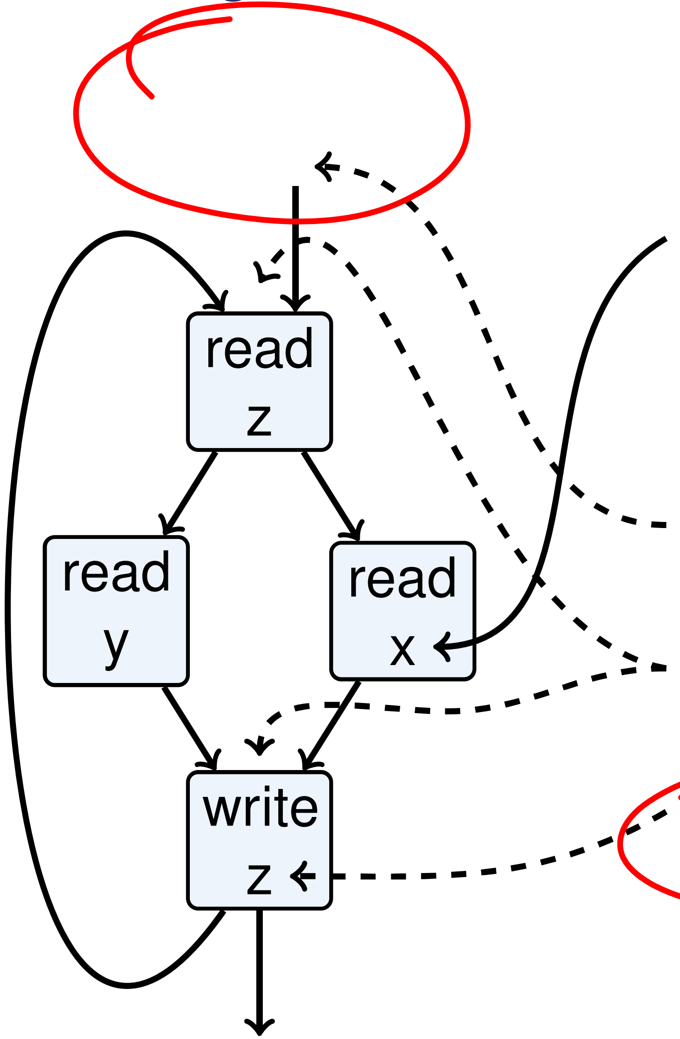
- Cache analyses almost exclusively for LRU
- In practice: FIFO, PLRU, . . .

Challenges for Cache Analysis



Always a cache hit/always a miss?

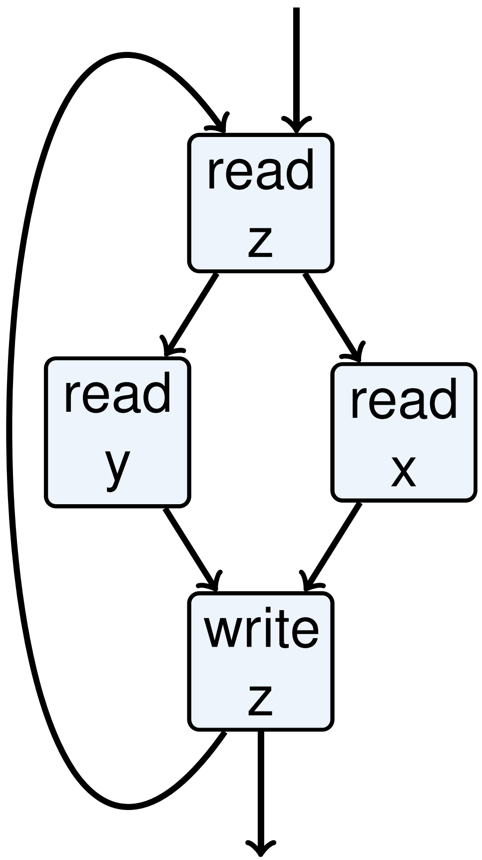
Challenges for Cache Analysis



Always a cache hit/always a miss?

1. Initial cache contents unknown.
2. Different paths lead to these points.
3. Cannot resolve address of *z*.

Deriving Invariants about Cache States using Abstract Interpretation



Collecting Semantics =
set of states at each program point that any execution may encounter there

Two approximations:

	Collecting Semantics	uncomputable
$\subseteq$	Cache Semantics	computable
$\subseteq$	γ(Abstract Cache Sem.)	efficiently computable

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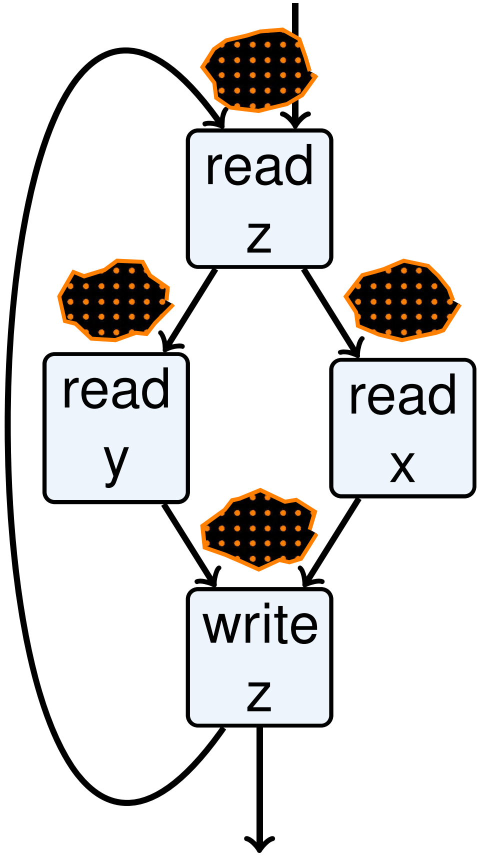

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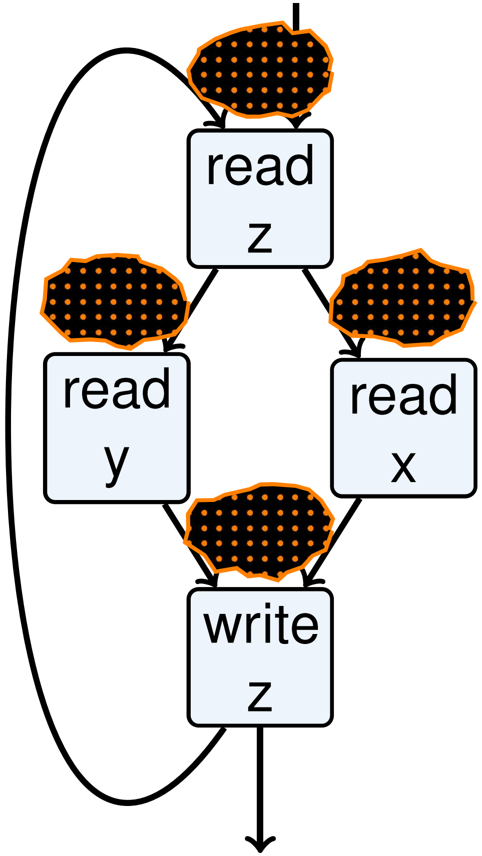

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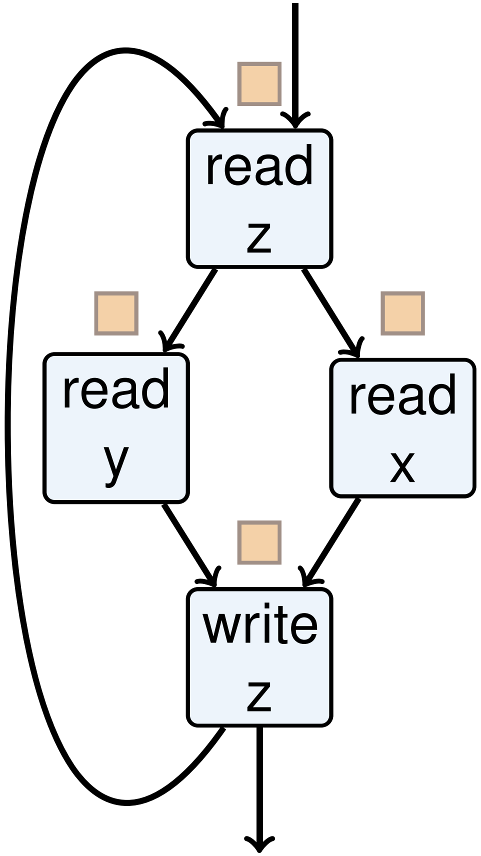

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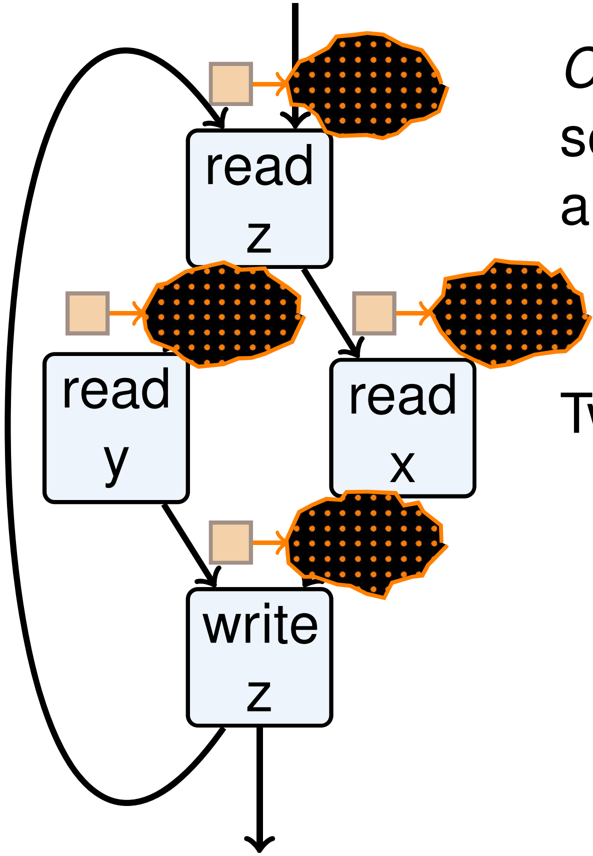

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Least-Recently-Used (LRU): Concrete Behavior

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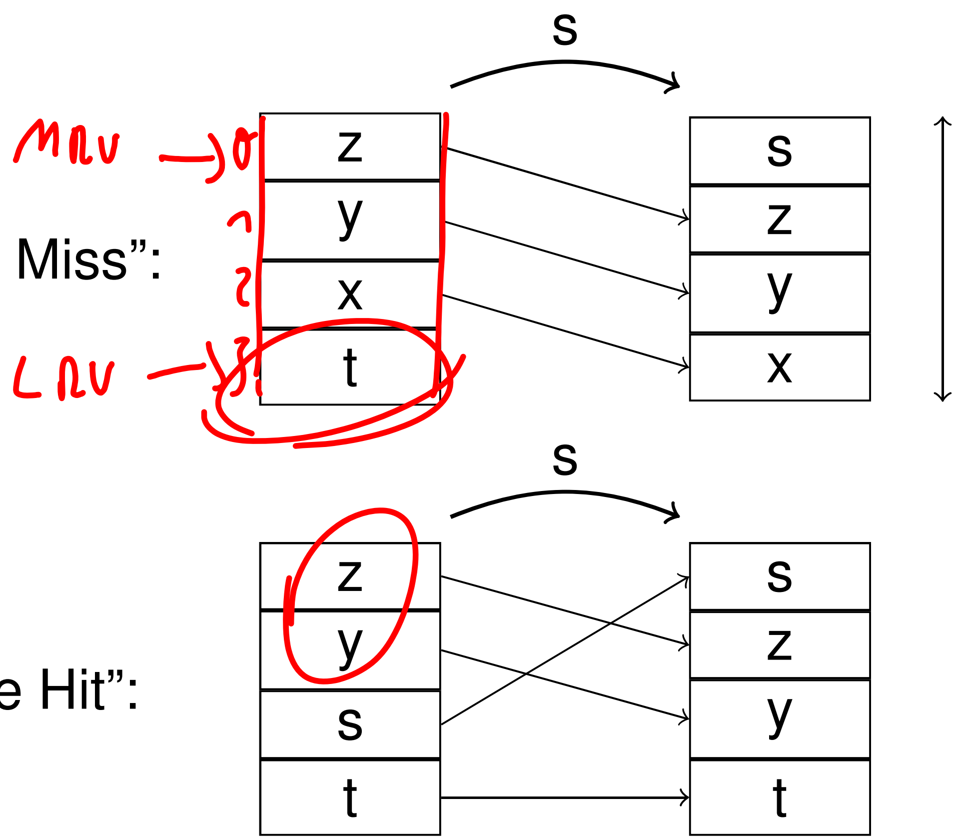
“Cache Miss”:

“Cache Hit”:



LRU has notion of age

LRU: How to predict cache hits?

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CONCRETE CACHE STATES

$C = \{1, \ldots, k\} \rightarrow B \cup \{\bot\}$

Ideas?

$C' = \{f : B \rightarrow \{1, \ldots, k, \infty\} \mid \forall a, b \in B : f(a) = f(b) \wedge f(a) \neq \infty \rightarrow a = b\}$

$A' = B \rightarrow \{1, \ldots, k, \infty\}$ | $A = \{1, \ldots, k\} \rightarrow \mathcal{P}(B)$

$\gamma(a^\#) = \{f \in C' \mid \forall b \in B.\ f(b) \leq a^\#(b)\}$

LRU: Must-Analysis: Abstract Domain

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- Used to predict *cache hits*.
- Maintains *upper bounds on ages* of memory blocks.
- Upper bound $\leq$ associativity $\longrightarrow$ memory block definitely cached.

Example

Abstract state:

{x}	age 0
{}	1
{s,t}	2
{}	age 3

. . . and its interpretation:

Describes the set of all concrete cache states in which x, s, and t occur,

- x with an age of 0,
- s and t with an age not older than 2.

$$\gamma([\{x\},\{\},\{s,t\},\{\}]) = \{[x,s,t,a],[x,t,s,a],[x,s,t,b],\ldots\}$$

Sound Update – Local Consistency

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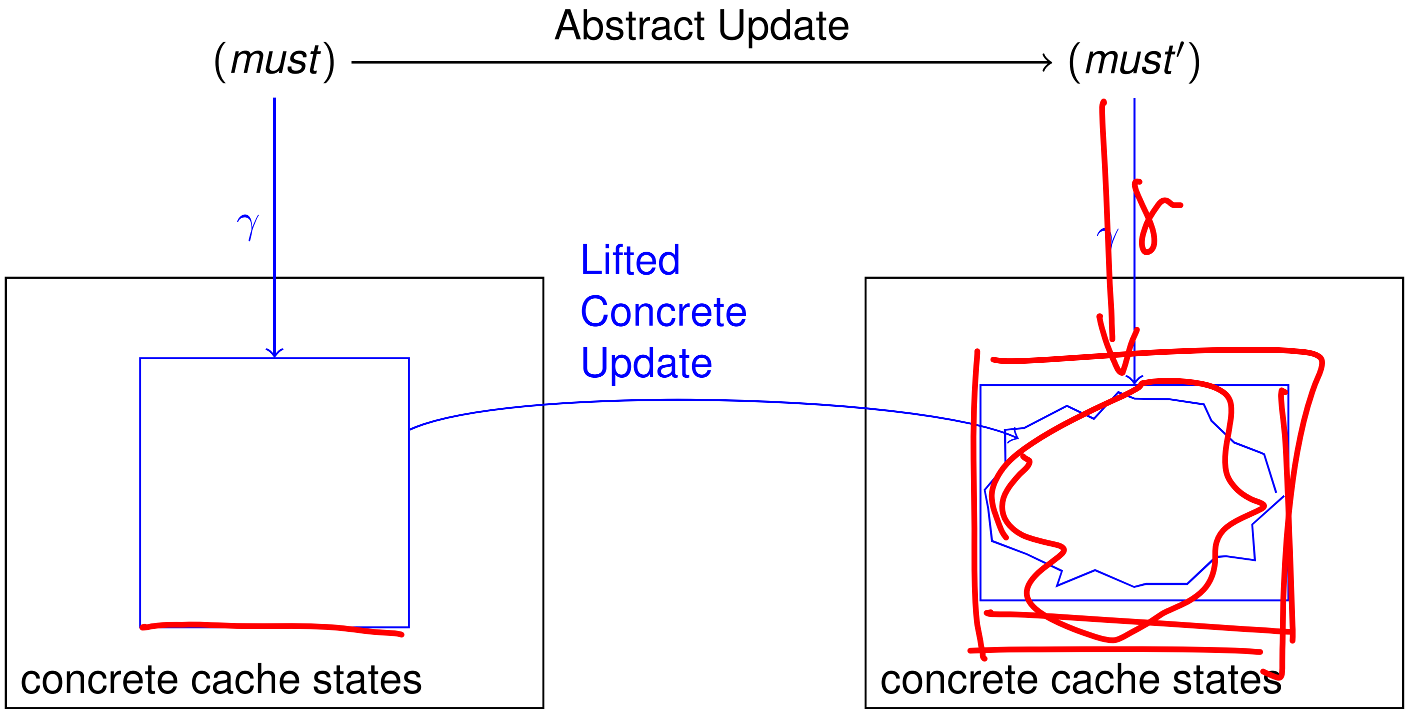
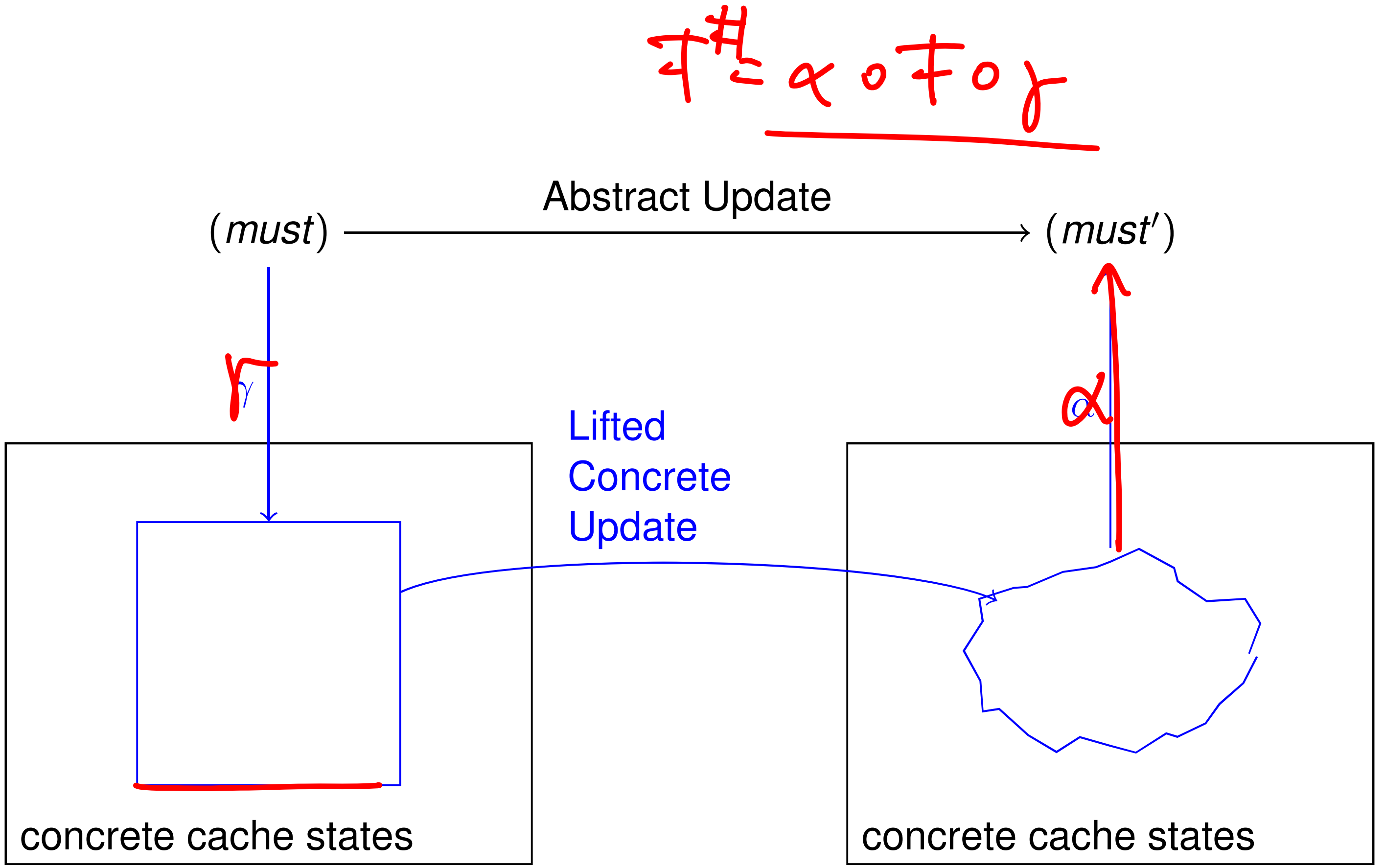


Sound Update – Best Abstract Transformer



Abstraction Function for Must-Analysis

1. What should the abstraction function α be?
2. Do α and γ form a Galois connection?

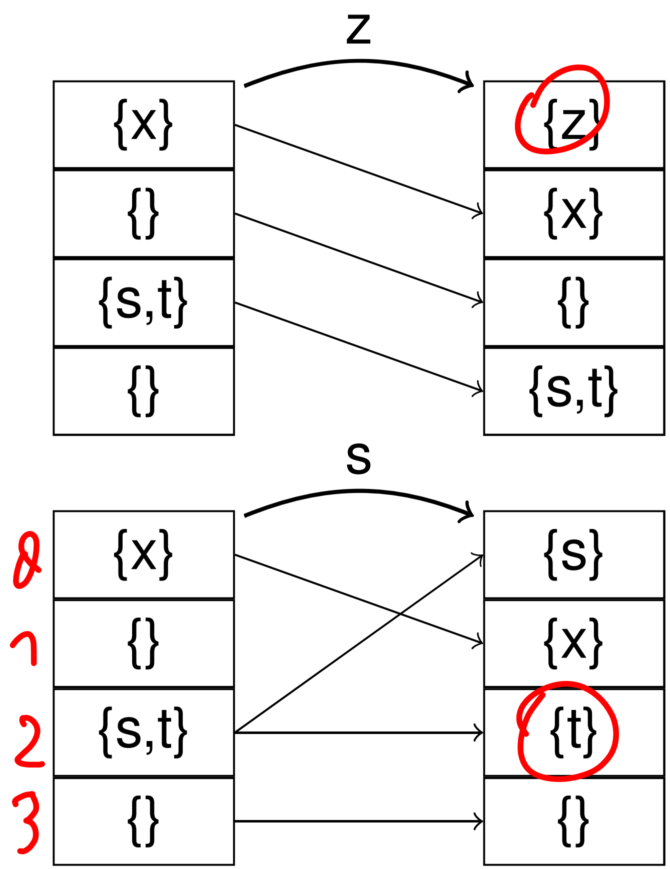
1. $\alpha(F) = \lambda b \in B. \max_{f \in F} f(b)$

2. ✓

LRU: Must-Analysis: Update

“Potential Cache Miss”:

“Definite Cache Hit”:



Why does *t* not age in the second case?

LRU: Must-Analysis: Join

Need to combine information where control-flow merges.

Join should be conservative (ensures γ is monotone):

- $\gamma(A) \subseteq \gamma(A \sqcup B)$
- $\gamma(B) \subseteq \gamma(A \sqcup B)$

{a}		{c}		{}
{}	$\sqcup$	{e}	$=$	{}
{c,f}		{a}		{a,c}
{d}		{d}		{d}

$e \mapsto \infty$

"Intersection + Maximal Age"

$$(a^\# \sqcup b^\#)(m) = \max\{a^\#(m), b^\#(m)\}$$

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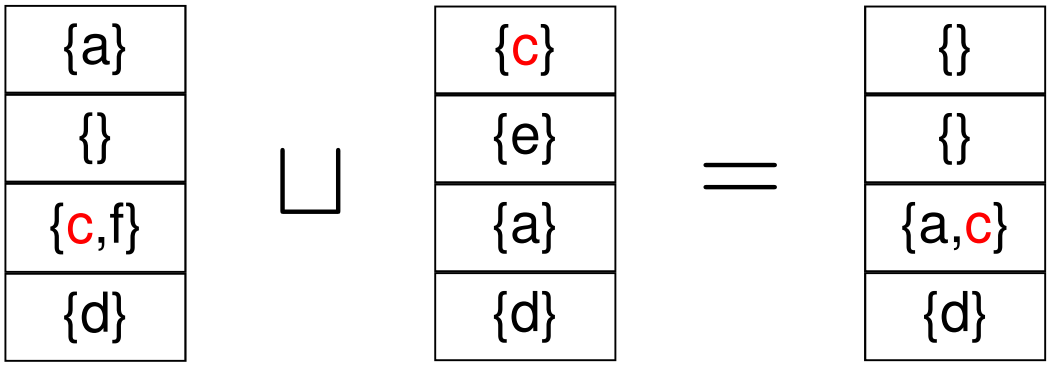

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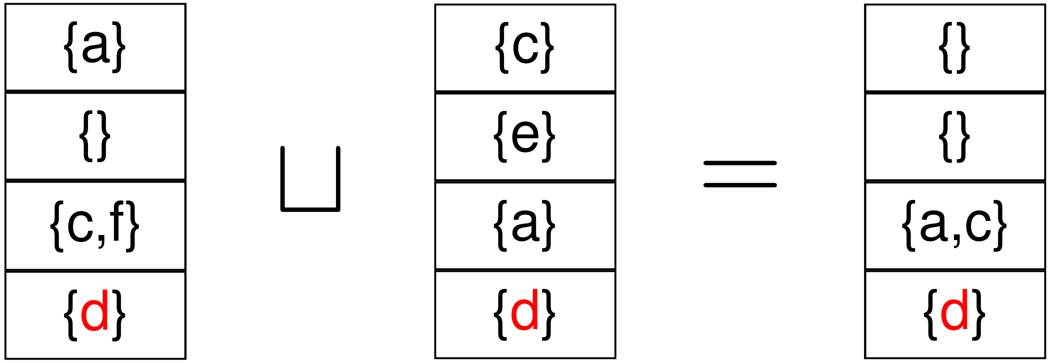

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"Intersection + Maximal Age"

How many memory blocks can be in the must-cache? $\rightarrow k$

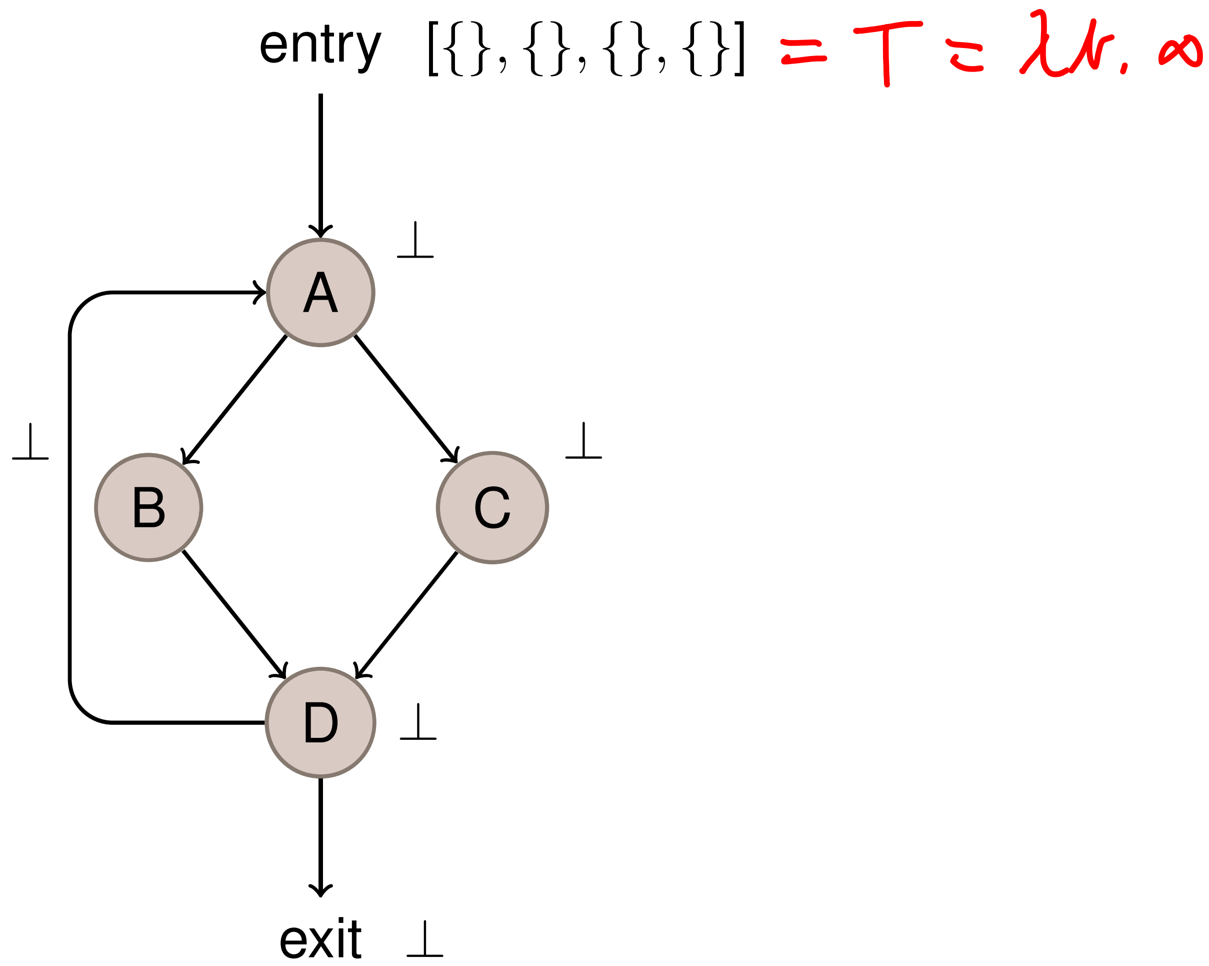
LRU: Must-Analysis: Ascending Chain Condition?

1. Remember connection between $\sqsubseteq$ and $\sqcup$.
2. Does the ascending chain condition hold?

1. $A \sqsubseteq B \iff A \sqcup B = B$.

2. ✓ HEIGHT OF LATTICE $\leq k^2$

Example: Must-Analysis



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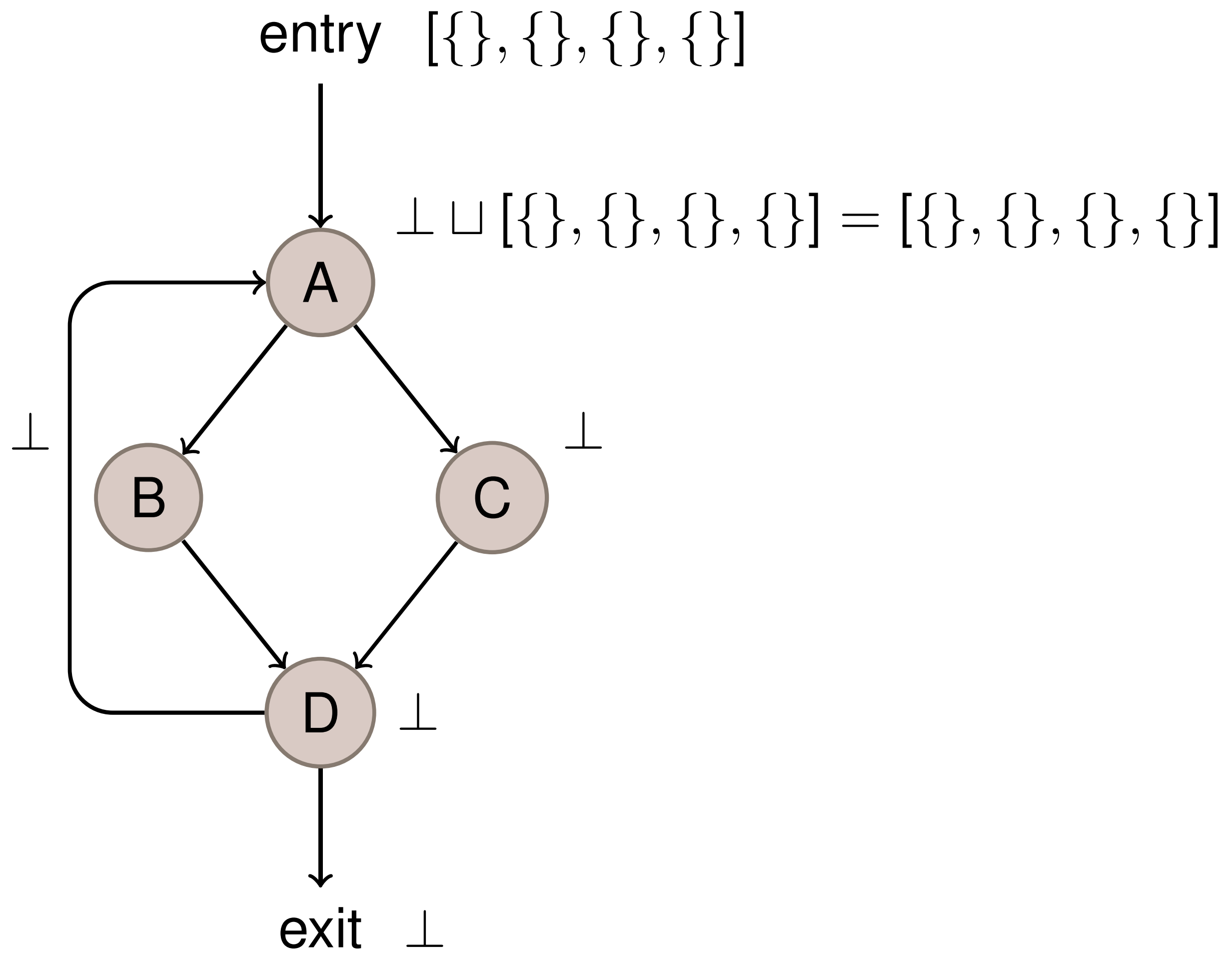

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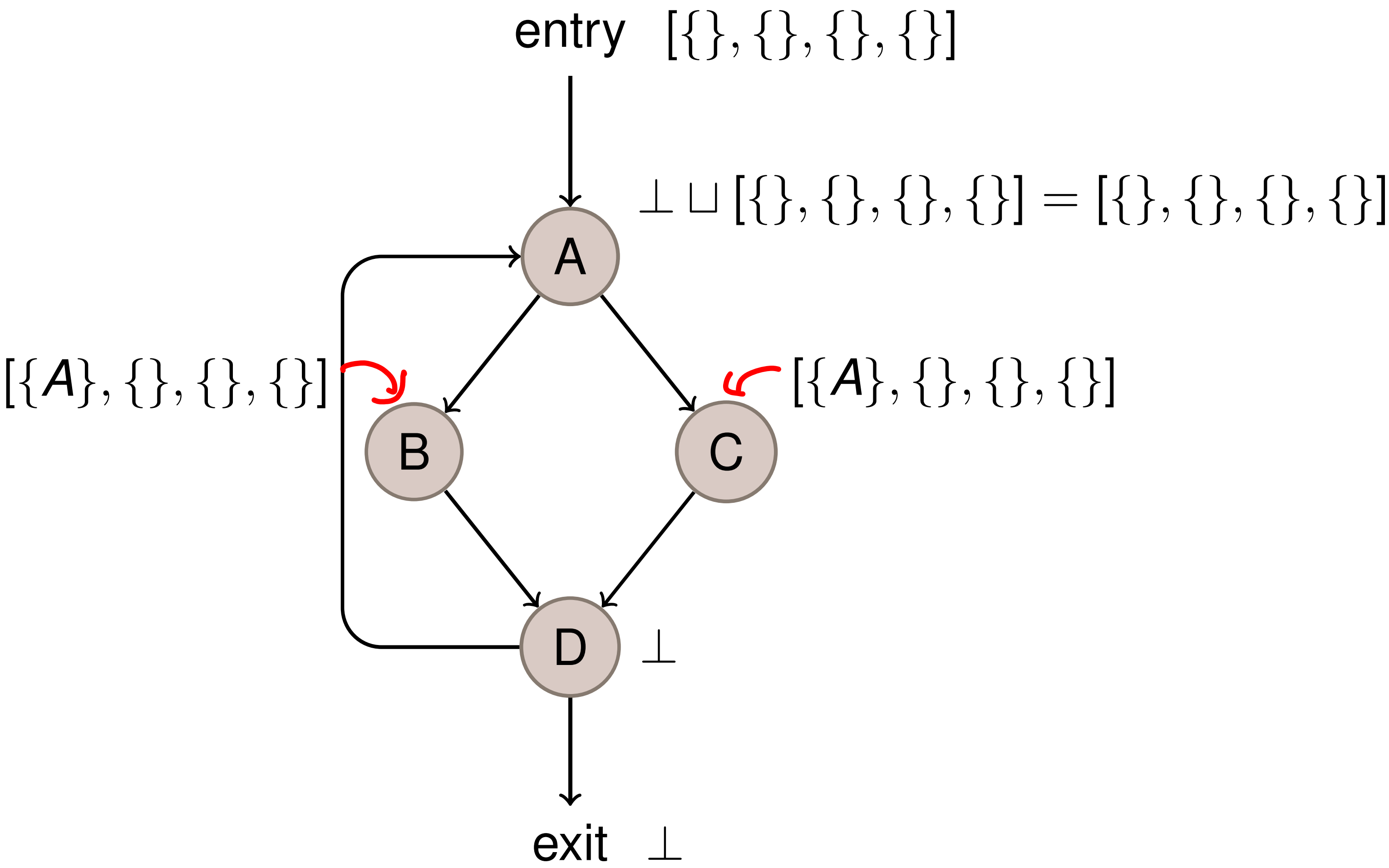

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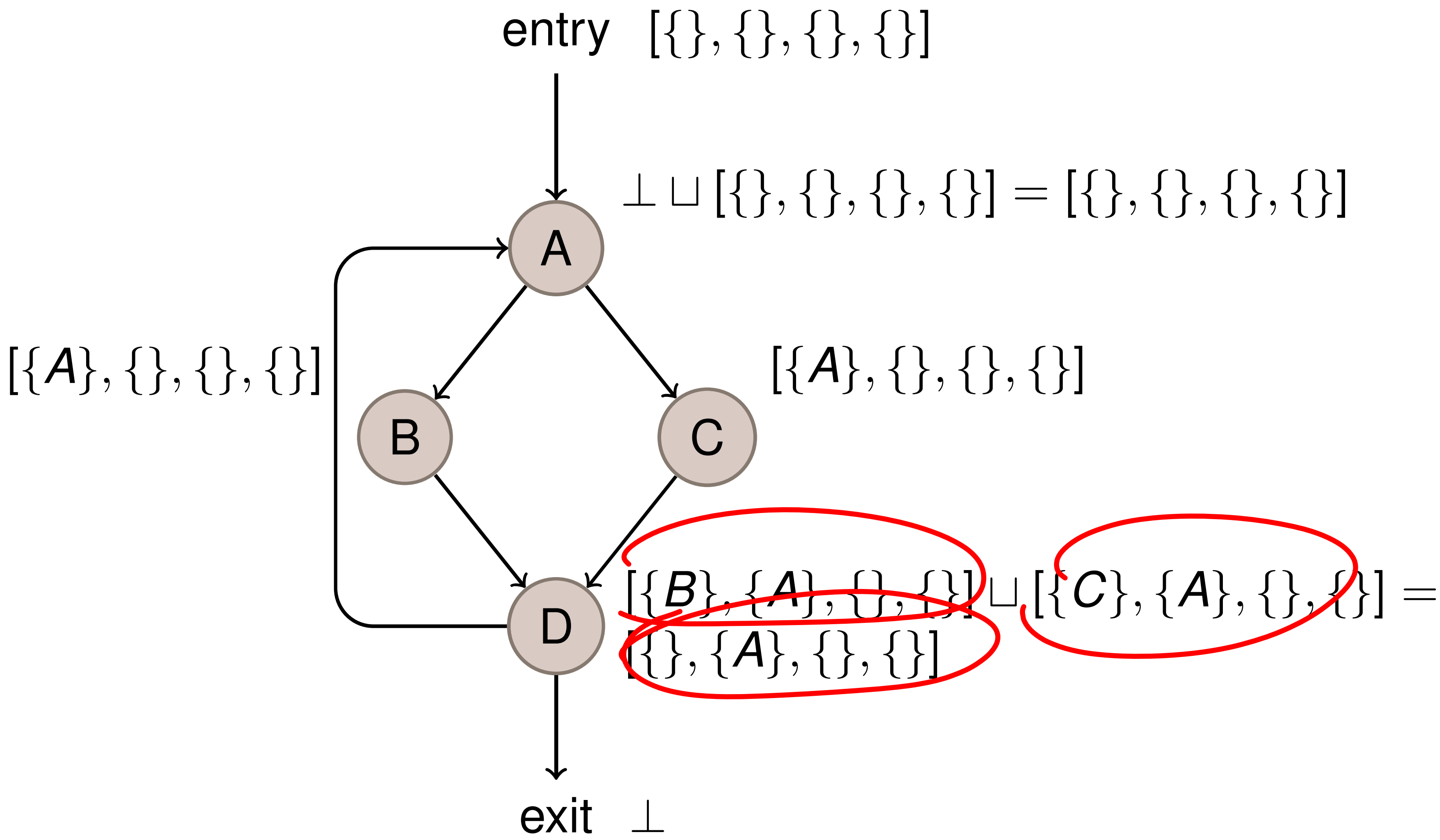

Example: Must-Analysis

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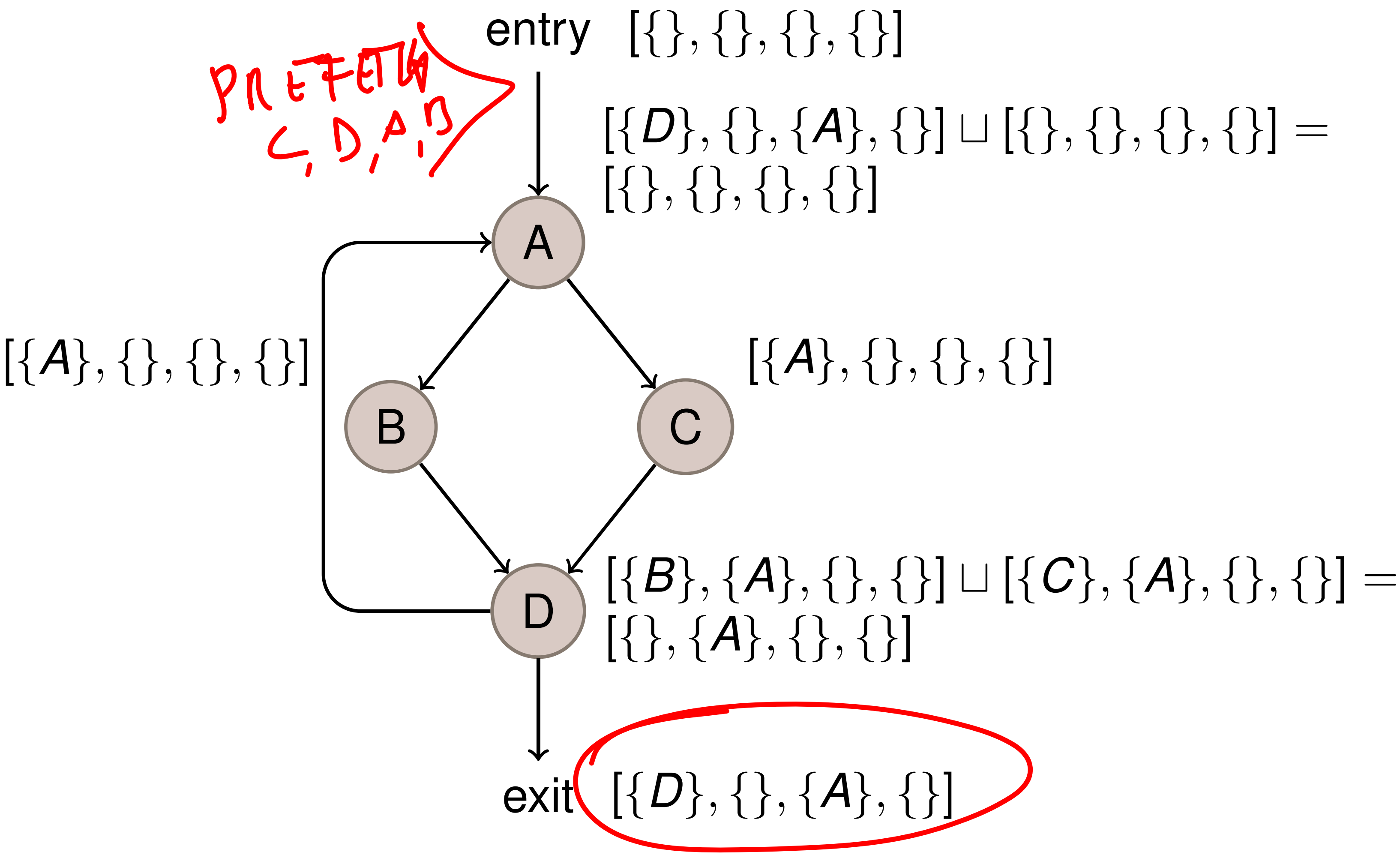


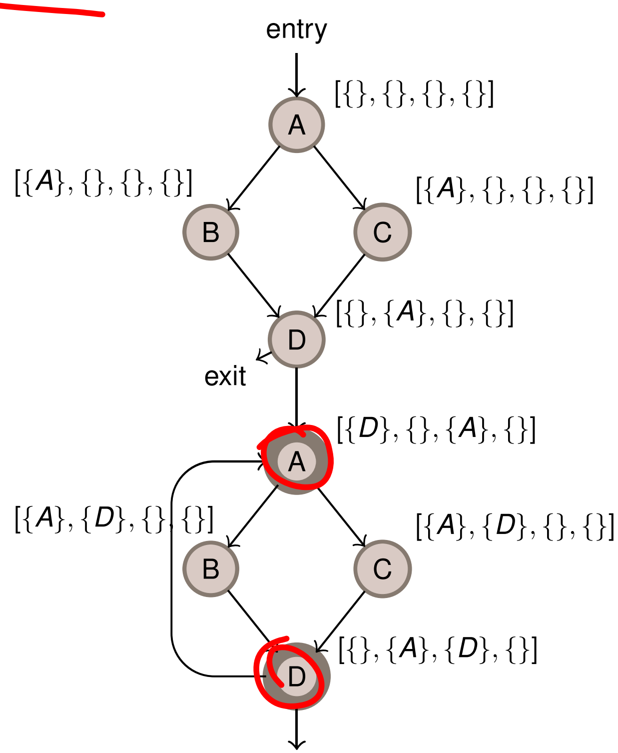
No cache hits can be predicted :-(

Context-Sensitive Analysis/Virtual Loop-Unrolling

- Problem:
  - The first iteration of a loop will always result in cache misses.
  - Similarly for the first execution of a function.
- Solution:
  - Virtually Unroll Loops: Distinguish the first iteration from others
  - Distinguish function calls by calling context.

Virtually unrolling the loop once:

- Accesses to A and D are provably hits after the first iteration
- Accesses to B and C can still not be classified. Within each execution of the loop, they may only miss once.
  $\longrightarrow$ Persistence Analysis



LRU: May-Analysis: Abstract Domain

- Used to predict *cache misses*.
- Maintains *lower bounds on ages* of memory blocks.
- Lower bound $\geq$ associativity
  $\longrightarrow$ memory block definitely *not* cached.

Example

Abstract state:

{x,y}	age 0
{}	
{s,t}	
{u}	age 3

...and its interpretation:

Describes the set of all concrete cache states in which no memory blocks except *x*, *y*, *s*, *t*, and *u* occur,

- *x* and *y* with an age of at least 0,
- *s* and *t* with an age of at least 2,
- *u* with an age of at least 3.

$$\gamma([\{x, y\}, \{\}, \{s, t\}, \{u\}]) = \{[x, y, s, t], [y, x, s, t], [x, y, s, u], \ldots\}$$

Abstraction Function for May-Analysis

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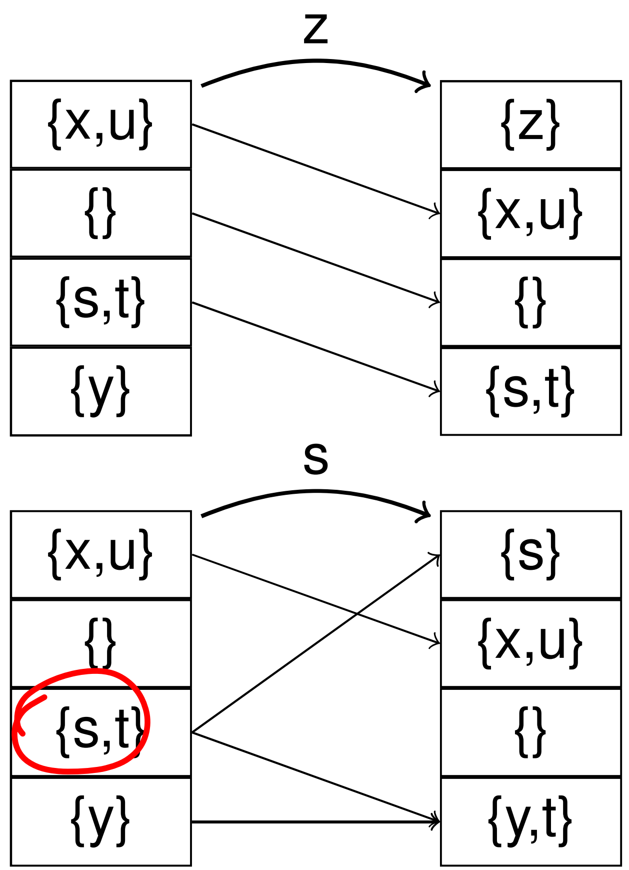
1. $\alpha(\mathcal{F}) = \lambda b.\ \min_{f \in \mathcal{F}} f(b)$

2. ✓

LRU: May-Analysis: Update

“Definite Cache Miss”:

“Potential Cache Hit”:



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LRU: May-Analysis: Join

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"Union + Minimal Age"

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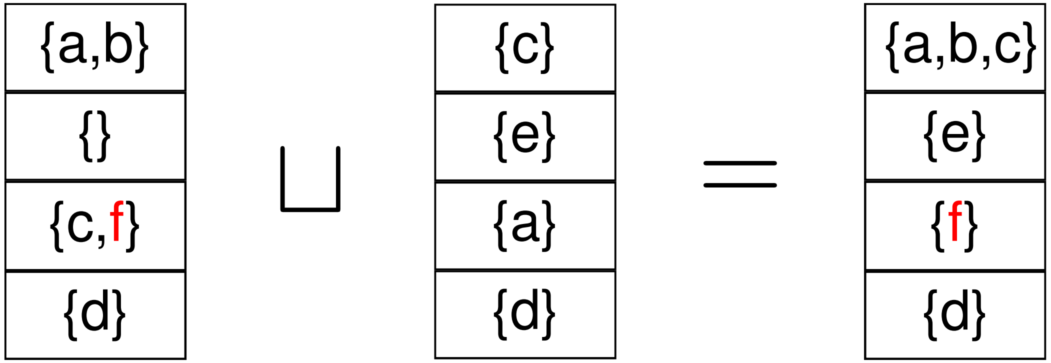

"Union + Minimal Age"

LRU: May-Analysis: Ascending Chain Condition?

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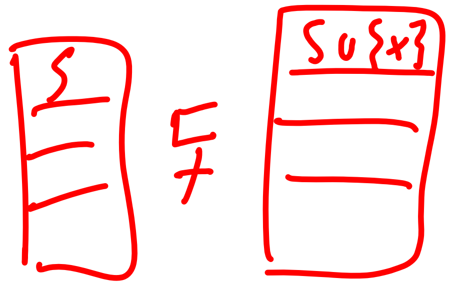
1. Does the ascending chain condition hold?
2. Does it matter in practice?

2. a) INSTRUCTION ACCESSES
→ NO "THEORETICAL" PROBLEM
b) DATA ACCESSES
→ DEPENDS.



Notion of Persistence

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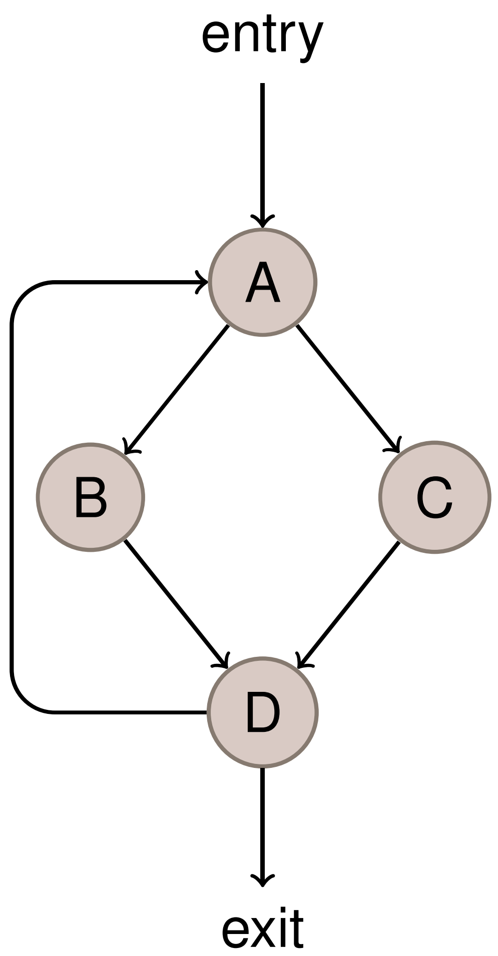
- Intuition: "Block *b* is *persistent* if it can only cause one cache miss in any execution."
- What is an appropriate concrete semantics that captures this property?
- Ideas for abstractions?

⇒ NEED "TRACE" SEMANTICS



Outline

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1 Caches

2 Cache Analysis for Least-Recently-Used

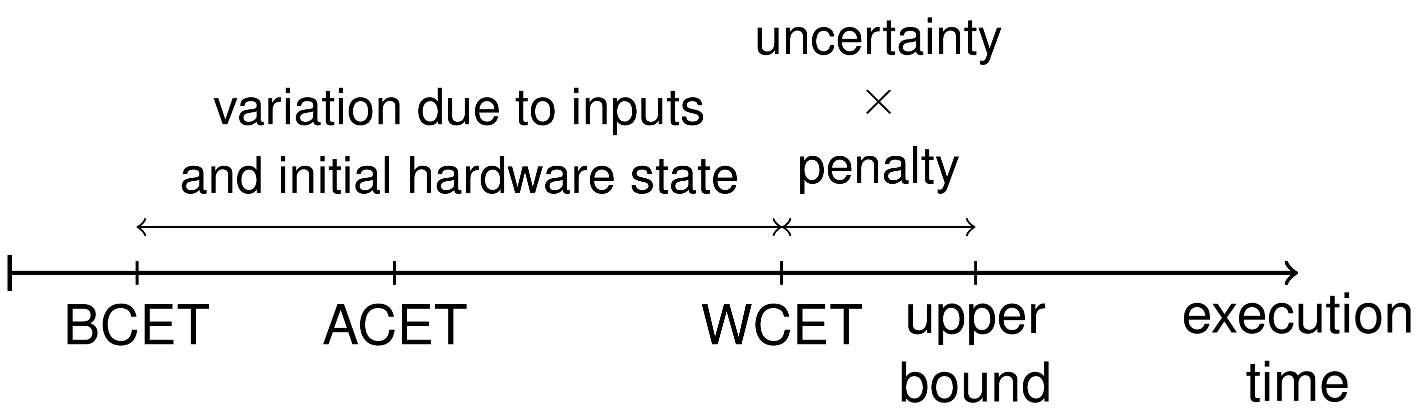
3 Beyond Least-Recently-Used
- Predictability Metrics
- Relative Competitiveness
- Sensitivity – Caches and Measurement-Based Timing Analysis

4 Summary

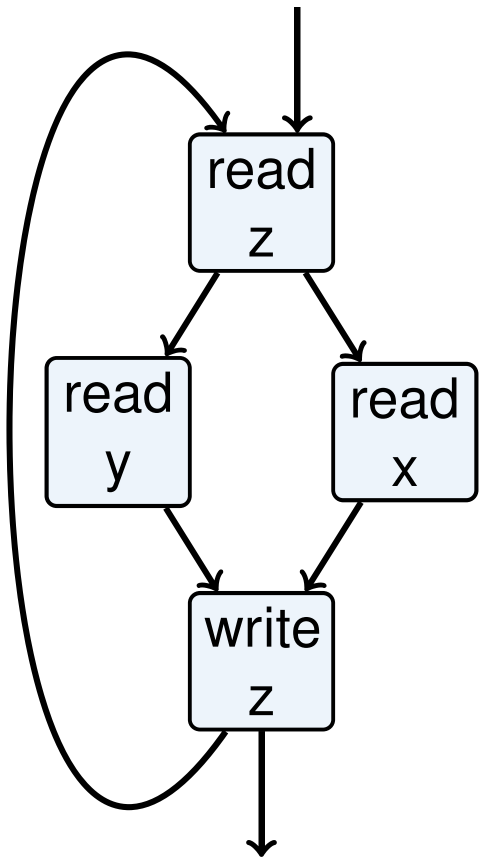
Outline

Uncertainty in WCET Analysis

- Amount of uncertainty determines precision of WCET analysis
- Uncertainty in cache analysis depends on replacement policy



Uncertainty in Cache Analysis



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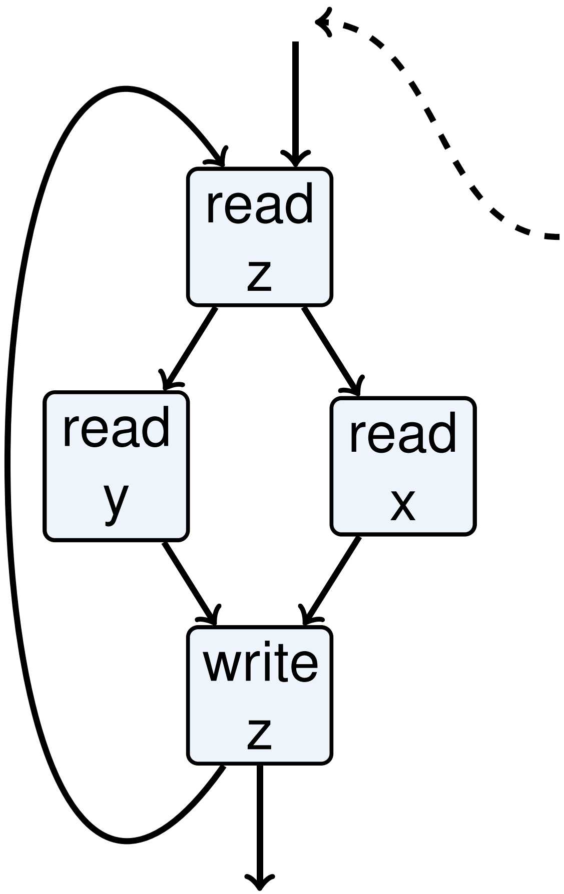
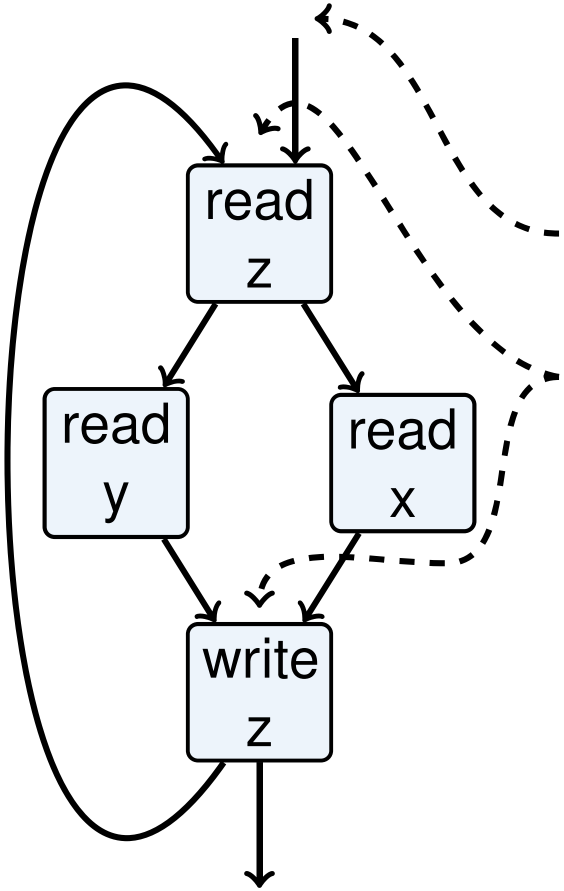


1. Initial cache contents unknown.

Uncertainty in Cache Analysis



1. Initial cache contents unknown.
2. Need to combine information.

Uncertainty in Cache Analysis

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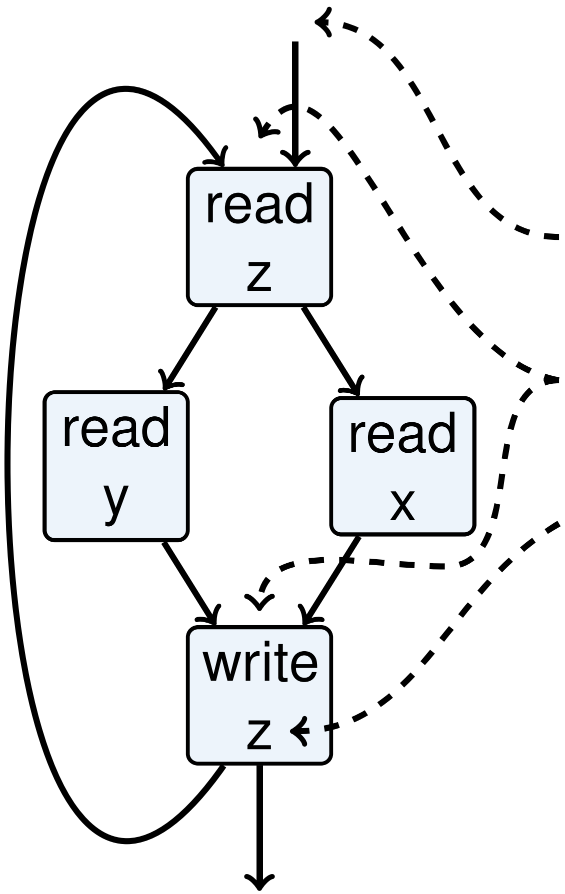

1. Initial cache contents unknown.
2. Need to combine information.
3. Cannot resolve address of *z*.

Uncertainty in Cache Analysis

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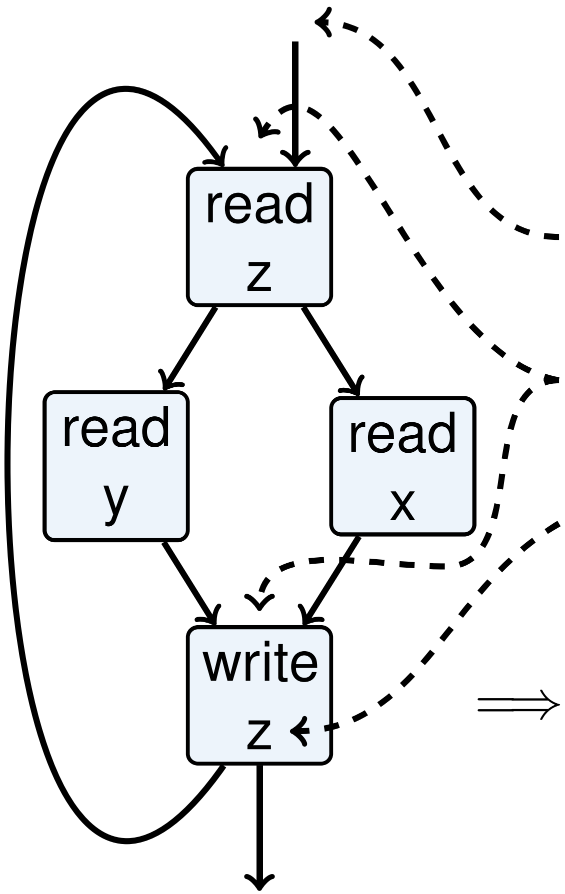

1. Initial cache contents unknown.
2. Need to combine information.
3. Cannot resolve address of z.

$\Longrightarrow$ Amount of uncertainty determined by ability to recover information

Predictability Metrics

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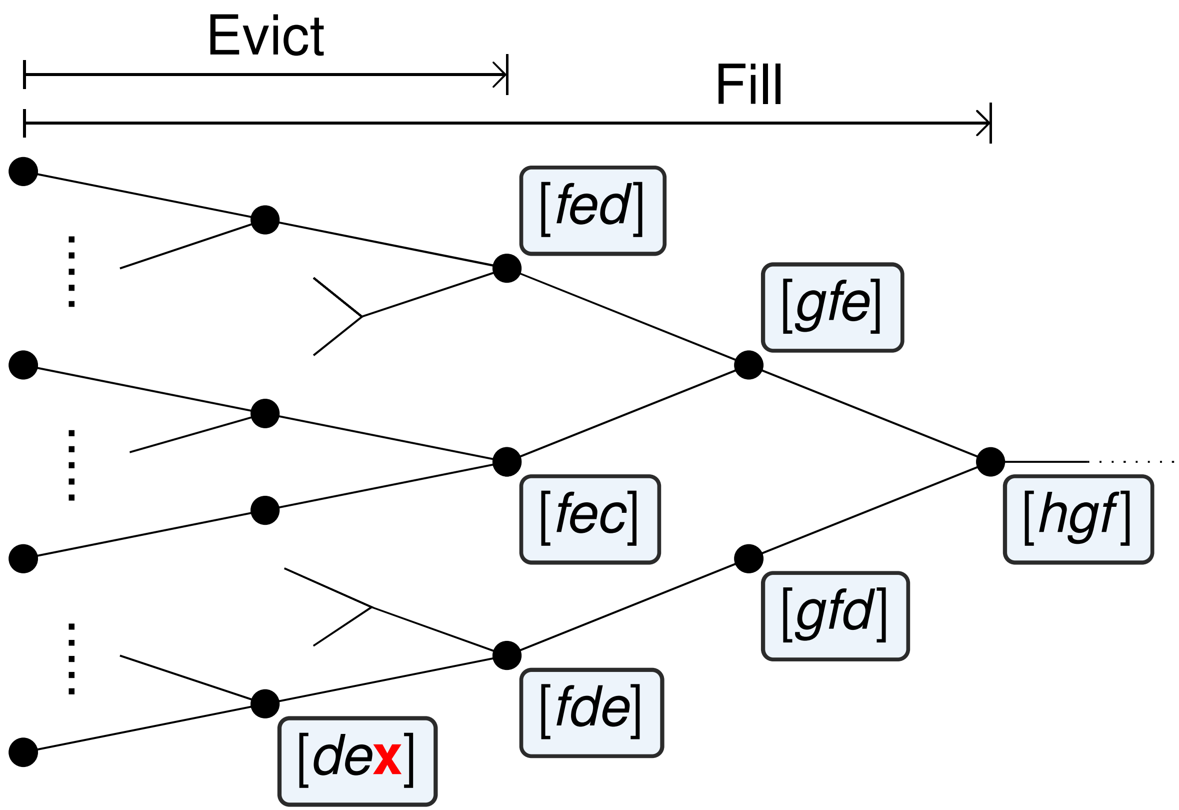


Sequence: $\langle$a, . . . , e, f, g, h$\rangle$

Meaning of Metrics

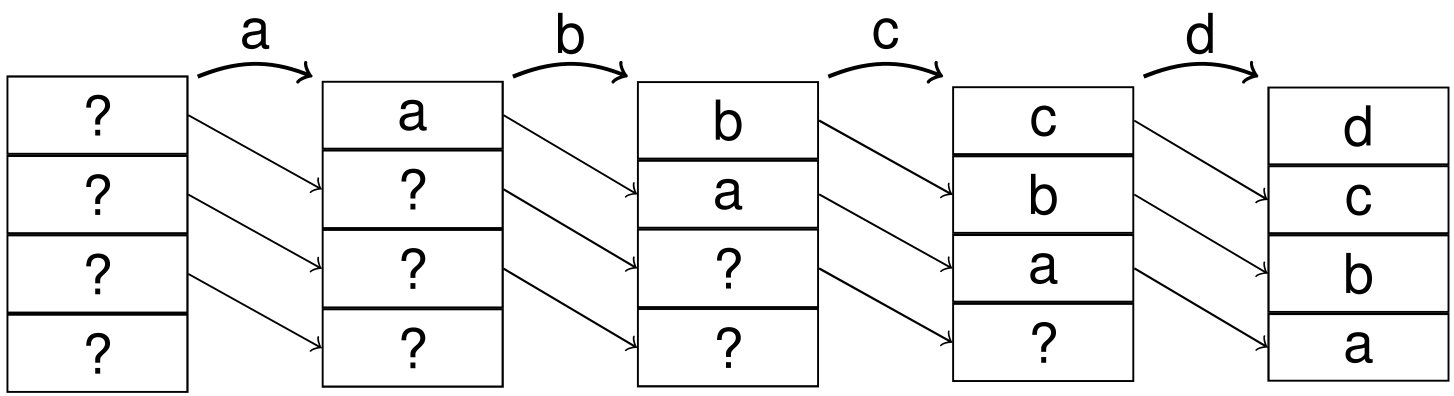
- Evict
  - Number of accesses to obtain *any may*-information.
  - I.e. when can an analysis predict any cache misses?
- Fill
  - Number of accesses to complete *may*- and *must*-information.
  - I.e. when can an analysis predict each access?

$\longrightarrow$ Evict and Fill bound the precision of *any* static cache analysis.

Can thus serve as a benchmark for analyses.

Evaluation of Least-Recently-Used

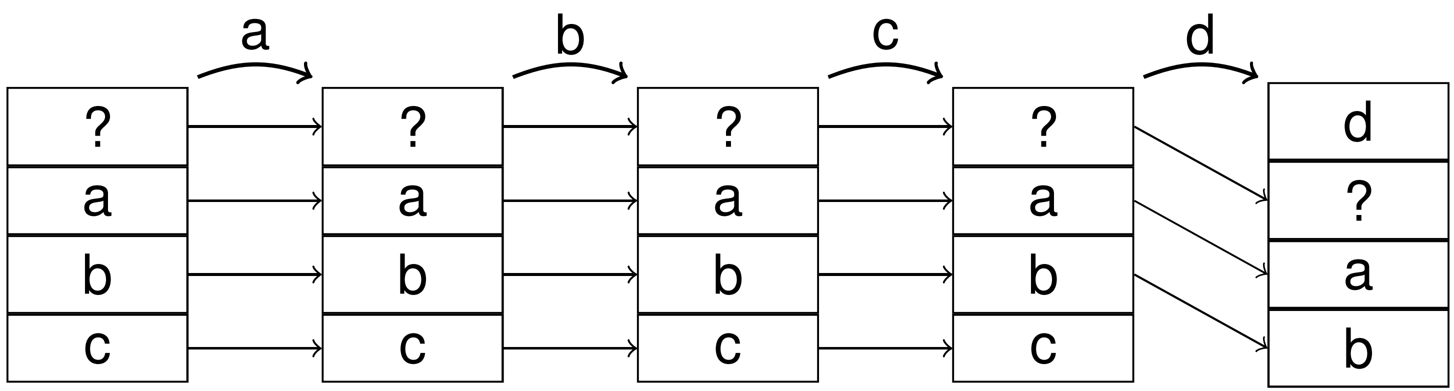
- LRU "forgets" about past quickly:
  - cares about most-recent access to each block only
  - order of previous accesses irrelevant



- In the example: Evict $=$ Fill $= 4$
- In general: Evict(k) $=$ Fill(k) $= k$, where k is the associativity of the cache

Evaluation of First-In First-Out (sketch)

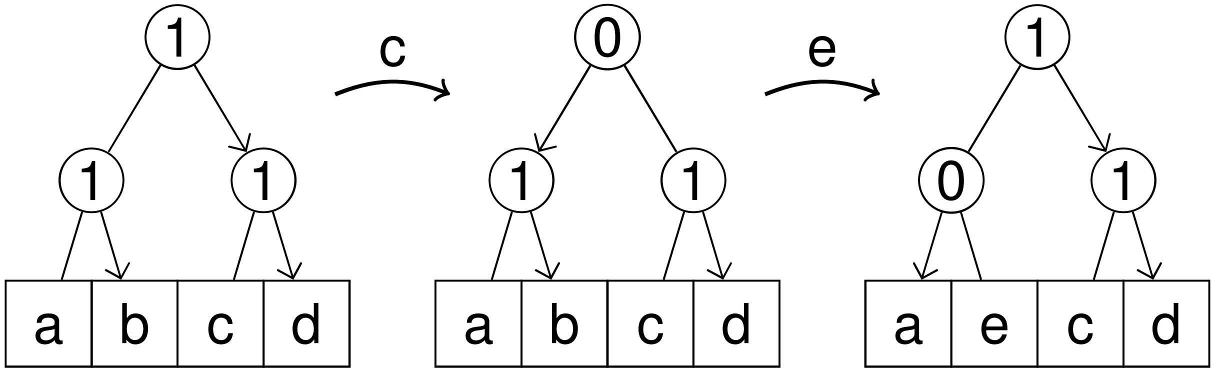
- Like LRU in the miss-case
- But: "Ignores" hits



- In the worst-case $k - 1$ hits and k misses: (k = associativity)
  $\longrightarrow$ Evict$(k) = 2k - 1$
- Another k accesses to obtain complete knowledge:
  $\longrightarrow$ Fill$(k) = 3k - 1$

Evaluation of Pseudo-LRU (sketch)

- Tree-bits point to block to be replaced



- Accesses “rejuvenate” neighborhood
  - Active blocks keep their (inactive) neighborhood in the cache
- Analysis yields:
  - $\text{Evict}(k) = \frac{k}{2} \log_2 k + 1$
  - $\text{Fill}(k) = \frac{k}{2} \log_2 k + k - 1$

Evaluation of Policies

Policy	Evict(k)	Fill(k)	Evict(8)	Fill(8)
LRU	k	k	8	8
FIFO	$2k-1$	$3k-1$	15	23
MRU	$2k-2$	$\infty/3k-4$	14	$\infty/20$
PLRU	$\frac{k}{2}\log_2 k+1$	$\frac{k}{2}\log_2 k+k-1$	13	19

- LRU is optimal w.r.t. metrics.
- Other policies are much less predictable.

$\longrightarrow$ Use LRU if predictability is a concern.

- How to obtain *may*- and *must*-information within the given limits for other policies?

Outline

Relative Competitiveness

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- Competitiveness (Sleator and Tarjan, 1985):
  worst-case performance of an online policy *relative to the optimal offline policy*
  - used to evaluate online policies
- Relative competitiveness (Reineke and Grund, 2008):
  worst-case performance of an online policy *relative to another online policy*
  - used to derive local and global cache analyses

Definition – Relative Miss-Competitiveness

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Notation

$$m_{\mathbf{P}}(p, s) \quad = \quad \text{number of misses that policy } \mathbf{P} \text{ incurs on access sequence } s \in M^* \text{ starting in state } p \in C^{\mathbf{P}}$$

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Definition (Relative miss competitiveness)

Policy **P** is (k, c)-miss-competitive relative to policy **Q** if

$$m_{\mathbf{P}}(p, s) \leq k \cdot m_{\mathbf{Q}}(q, s) + c$$

for all access sequences $s \in M^*$ and cache-set states $p \in C^{\mathbf{P}}, q \in C^{\mathbf{Q}}$ that are compatible $p \sim q$.

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for all access sequences $s \in M^*$ and cache-set states $p \in C^{\mathbf{P}}, q \in C^{\mathbf{Q}}$ that are compatible $p \sim q$.

Definition (Competitive miss ratio of P relative to Q)

The smallest k, s.t. **P** is (k, c)-miss-competitive rel. to **Q** for some c.

Example – Relative Miss-Competitiveness

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P is $(3, 4)$-miss-competitive relative to **Q**.
If **Q** incurs x misses, then **P** incurs at most $3 \cdot x + 4$ misses.

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Worst: **P** is not-miss-competitive (or ∞-miss-competitive) relative to **Q**.

Example – Relative Hit-Competitiveness

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P is $(\frac{2}{3}, 3)$-hit-competitive relative to **Q**.
If **Q** has x hits, then **P** has at least $\frac{2}{3} \cdot x - 3$ hits.

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Best: **P** is $(1, 0)$-hit-competitive relative to **Q**.
Equivalent to $(1, 0)$-miss-competitiveness.

Worst: **P** is $(0, 0)$-hit-competitive relative to **Q**.
Analogue to ∞-miss-competitiveness.

Local Guarantees: $(1,0)$-Competitiveness

Let **P** be $(1,0)$-competitive relative to **Q**:

$$m_{\mathbf{P}}(p,s) \leq 1 \cdot m_{\mathbf{Q}}(q,s) + 0$$
$$\Leftrightarrow m_{\mathbf{P}}(p,s) \leq m_{\mathbf{Q}}(q,s)$$

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1. If **Q** “hits”, so does **P**, and
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$$m_{\mathbf{P}}(p,s) \leq 1 \cdot m_{\mathbf{Q}}(q,s) + 0$$
$$\Leftrightarrow m_{\mathbf{P}}(p,s) \leq m_{\mathbf{Q}}(q,s)$$

1. If **Q** “hits”, so does **P**, and
2. if **P** “misses”, so does **Q**.

As a consequence,

1. a *must*-analysis for **Q** is also a *must*-analysis for **P**, and
2. a *may*-analysis for **P** is also a *may*-analysis for **Q**.

Global Guarantees: (k, c)-Competitiveness

Given: Global guarantees for policy **Q**.
Wanted: Global guarantees for policy **P**.

Global Guarantees: (k, c)-Competitiveness

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Given: Global guarantees for policy **Q**.
Wanted: Global guarantees for policy **P**.

1. Determine competitiveness of policy **P** relative to policy **Q**.

$$\mathbf{m_P} \leq \mathbf{k} \cdot \mathbf{m_Q} + \mathbf{c}$$

Global Guarantees: (k, c)-Competitiveness

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2. Compute global guarantee for task T under policy **Q**.

$$\mathbf{m_Q(T)}$$

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$$\mathbf{m_P \leq k \cdot m_Q + c}$$

2. Compute global guarantee for task T under policy **Q**.

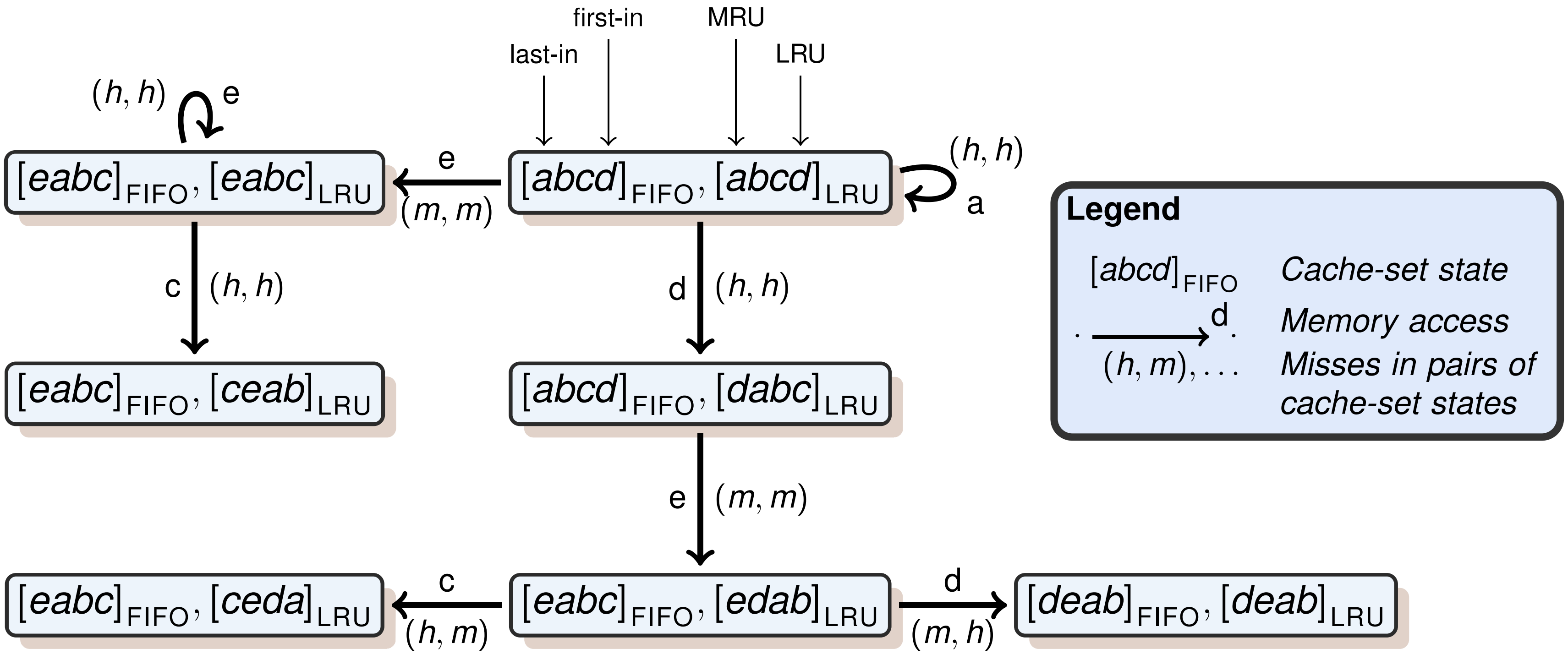
$$\mathbf{m_Q(T)}$$

3. Calculate global guarantee on the number of misses for **P** using the global guarantee for **Q** and the competitiveness results of **P** relative to **Q**.

$$\mathbf{m_P \leq k \cdot m_Q + c} \quad \mathbf{m_Q(T)} \quad = \quad \mathbf{m_P(T)}$$

Relative Competitiveness: Automatic Computation

P and **Q** (here: FIFO and LRU) induce transition system:

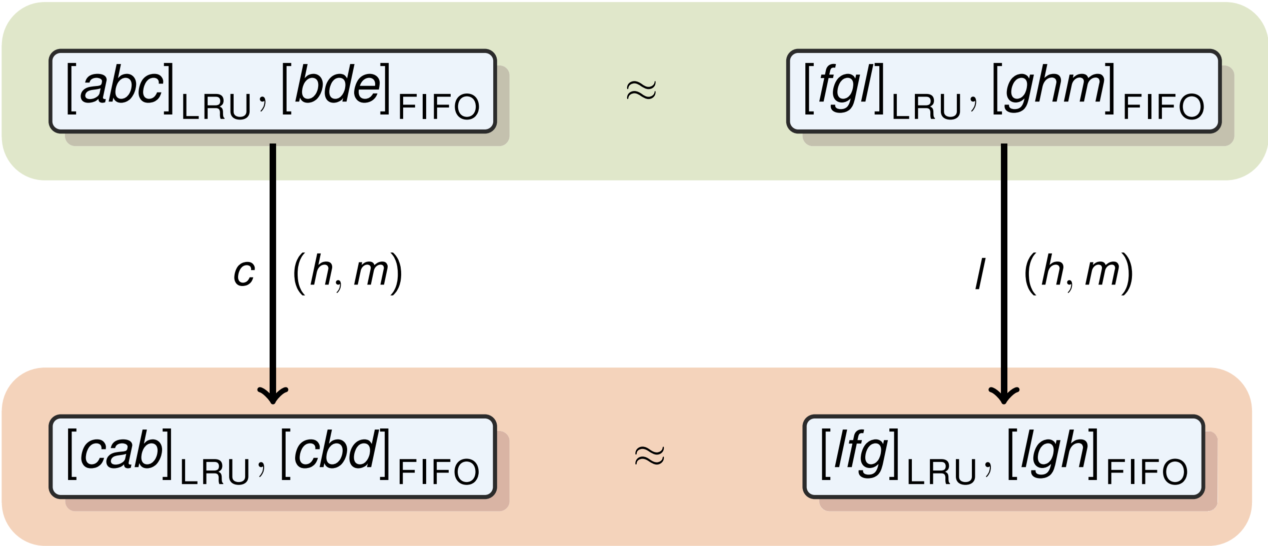


Competitive miss ratio = maximum ratio of misses in policy **P** to misses in policy **Q** in transition system

Transition System is ∞ Large

Problem: The induced transition system is ∞ large.

Observation: Only the *relative positions* of elements matter:



Solution: Construct *finite* quotient transition system.

≈-Equivalent States in Running Example

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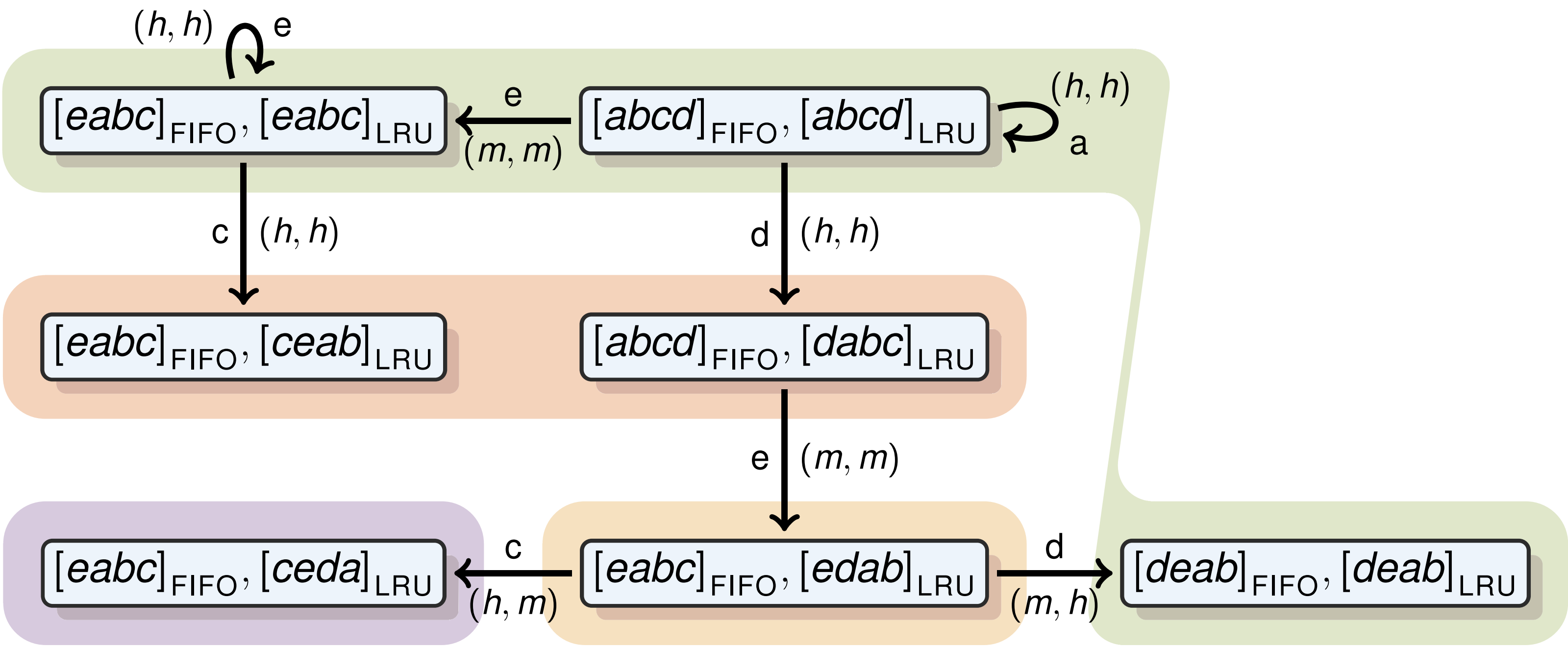
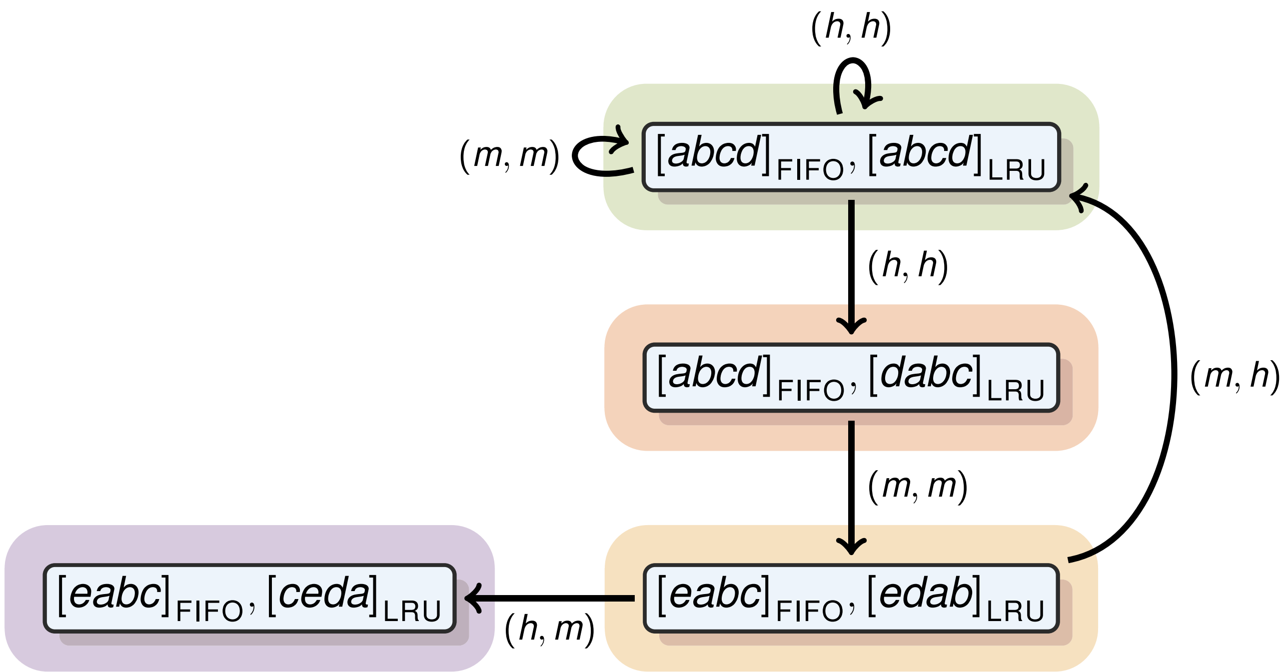


Finite Quotient Transition System

Merging $\approx$-equivalent states yields a finite quotient transition system:



Competitive Ratio = Maximum Cycle Ratio

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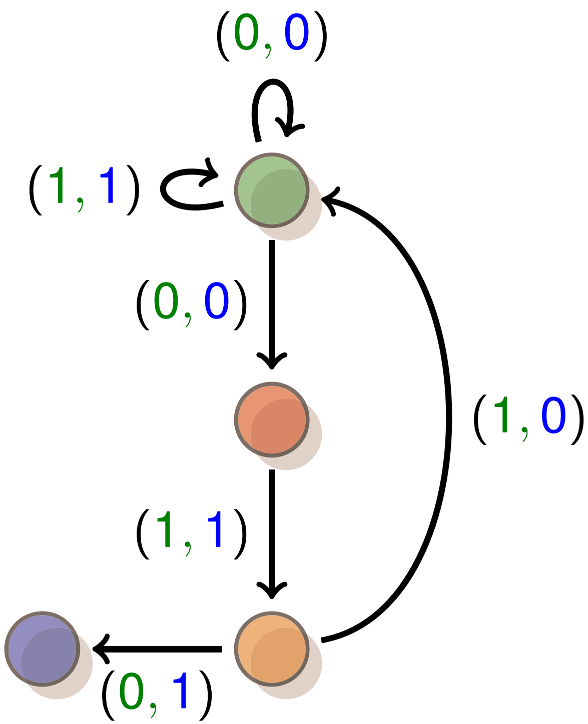
maximum ratio of misses in policy **P** to misses in policy **Q**



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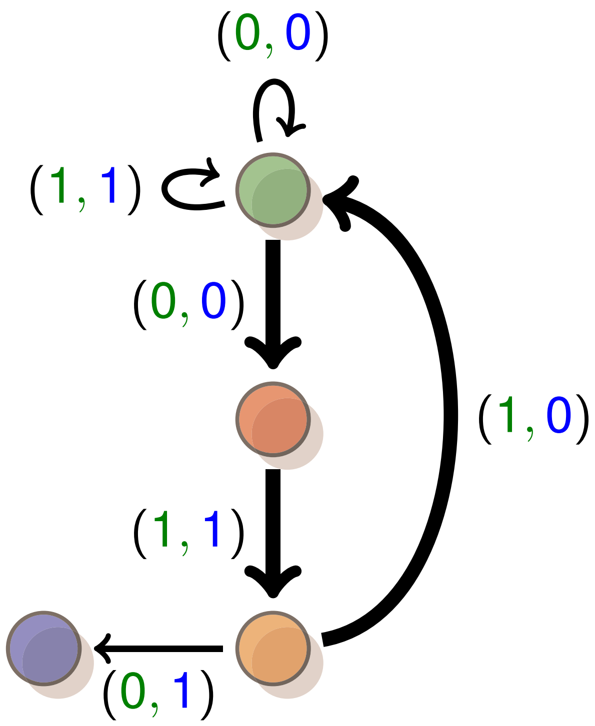

Maximum cycle ratio = $\frac{0+1+1}{0+1+0} = 2$

Tool Implementation

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- Implemented in Java, called Relacs
- Interface for replacement policies

- Fully automatic
- Provides example sequences for competitive ratio and constant

- Analysis usually practically feasible up to associativity 8
  - limited by memory consumption
  - depends on similarity of replacement policies

Online version:

`http://rw4.cs.uni-sb.de/~reineke/relacs`

Generalizations

Identified patterns and proved generalizations by hand.

Aided by example sequences generated by tool.

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$$\text{PLRU}(k) \text{ is } (1,0) \text{ comp. rel. to } \text{LRU}(1+\mathit{log}_2 k),$$

$$\longrightarrow \text{LRU-}\textit{must}\text{-analysis can be used for PLRU}$$

$$\text{FIFO}(k) \text{ is } (\tfrac{1}{2}, \tfrac{k-1}{2}) \text{ hit-comp. rel. to } \text{LRU}(k), \text{ whereas}$$

$$\text{LRU}(k) \text{ is } (0,0) \text{ hit-comp. rel. to } \text{FIFO}(k), \text{ but}$$

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$\text{FIFO}(k)$ is $(\frac{1}{2}, \frac{k-1}{2})$ hit-comp. rel. to $\text{LRU}(k)$, whereas
$\text{LRU}(k)$ is $(0,0)$ hit-comp. rel. to $\text{FIFO}(k)$, but

$\text{LRU}(2k-1)$ is $(1,0)$ comp. rel. to $\text{FIFO}(k)$, and
$\text{LRU}(2k-2)$ is $(1,0)$ comp. rel. to $\text{MRU}(k)$.

$\longrightarrow$ LRU-*may*-analysis can be used for FIFO and MRU
$\longrightarrow$ optimal with respect to predictability metric Evict

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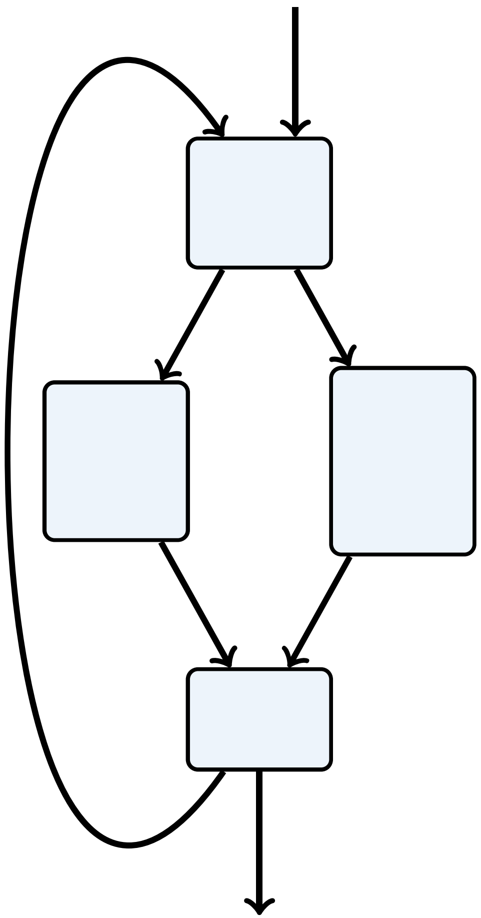
FIFO-*may*-analysis used in the analysis of the branch target buffer of the MOTOROLA POWERPC 56X.

Outline

Measurement-Based Timing Analysis

- Run program on a number of inputs and initial states.
- Combine measurements for basic blocks to obtain WCET estimation.
- Sensitivity Analysis demonstrates this approach may be dramatically wrong.



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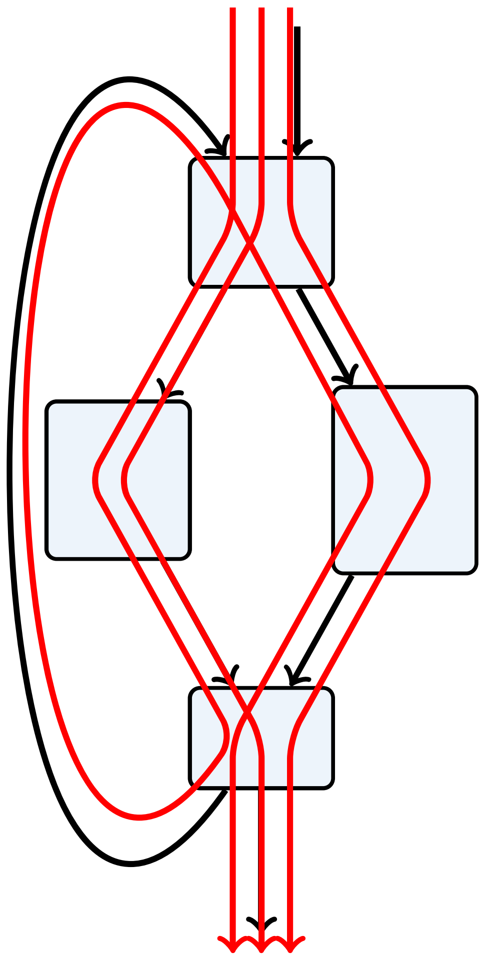
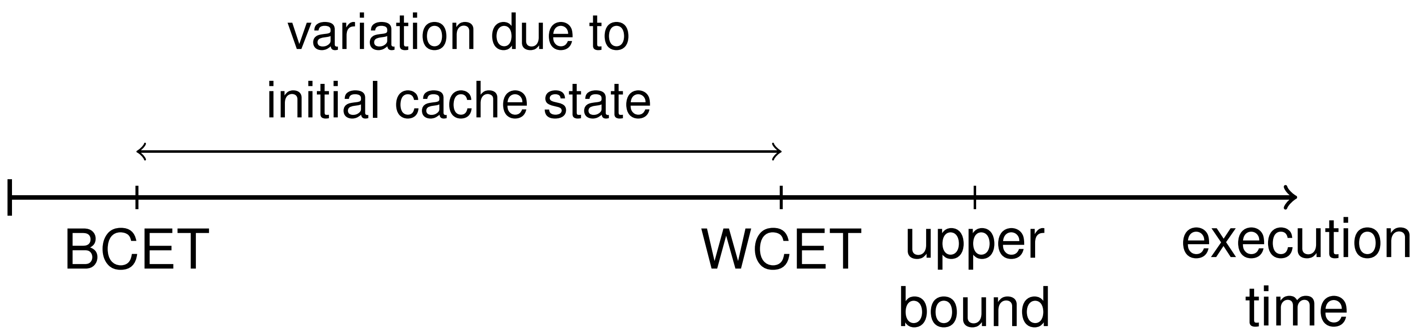


Influence of Initial Cache State



Definition (Miss sensitivity)

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$$m_{\mathbf{P}}(p, s) \leq k \cdot m_{\mathbf{P}}(p', s) + c$$

for all access sequences $s \in M^*$ and cache-set states $p, p' \in C^{\mathbf{P}}$.

Sensitivity Results

Policy	2	3	4	5	6	7	8
LRU	$1,2$	$1,3$	$1,4$	$1,5$	$1,6$	$1,7$	$1,8$
FIFO	$2,2$	$3,3$	$4,4$	$5,5$	$6,6$	$7,7$	$8,8$
PLRU	$1,2$	–	∞	–	–	–	∞
MRU	$1,2$	$3,4$	$5,6$	$7,8$	MEM	MEM	MEM

- LRU is optimal. Performance varies in the least possible way.
- For FIFO, PLRU, and MRU the number of misses may vary strongly.
- Case study based on simple model of execution time by Hennessy and Patterson (2003):
  WCET may be 3 times higher than a measured execution time for 4-way FIFO.

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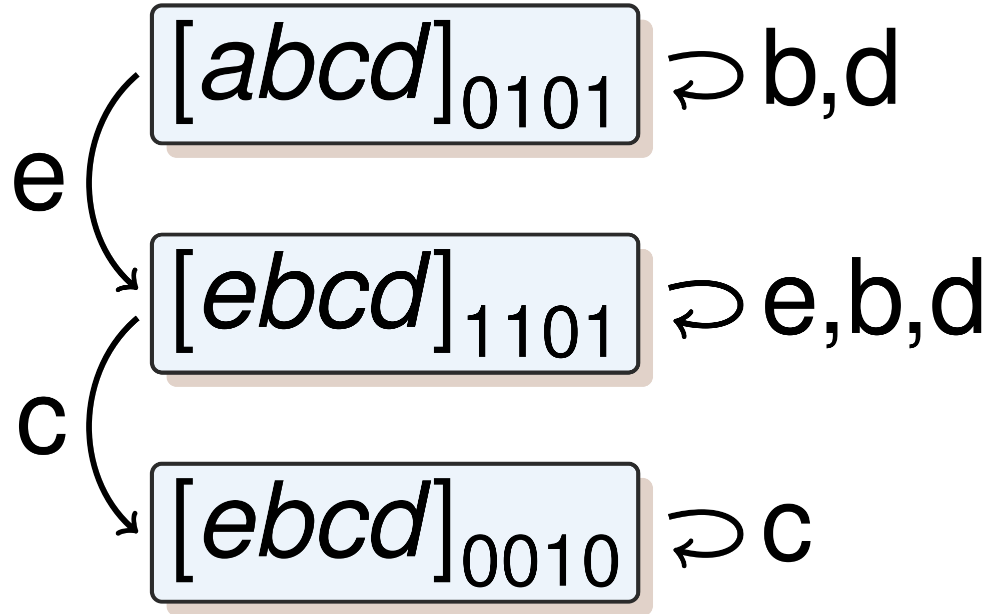
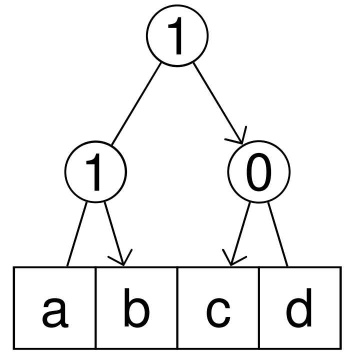
Most-Recently-Used – MRU

MRU-bits record whether line was recently used

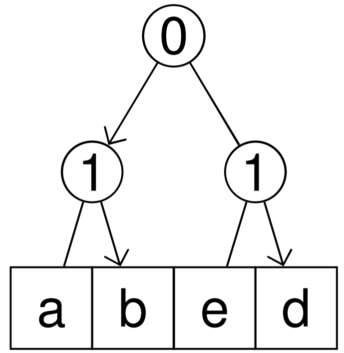


⟶ Never converges

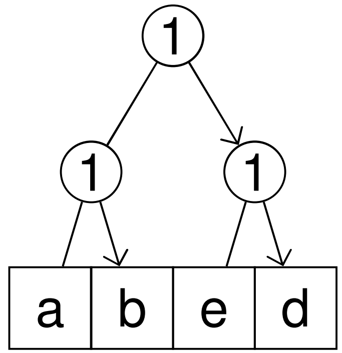
Pseudo-LRU – PLRU



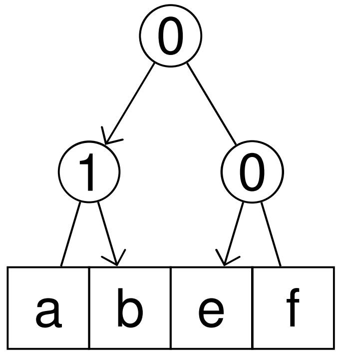
Initial cache-set state $[a, b, c, d]_{110}$.



After a miss on *e*. State: $[a, b, e, d]_{011}$.



After a hit on *a*. State: $[a, b, e, d]_{111}$.



After a miss on *f*. State: $[a, b, e, f]_{010}$.

Hit on *a* “rejuvenates” neighborhood; “saves” *b* from eviction.

May- and Must-Information

$$
\begin{aligned}
May^{\mathbf{P}}(s) &:= \bigcup_{p \in C^{\mathbf{P}}} CC_{\mathbf{P}}(update_{\mathbf{P}}(p, s)) \\
Must^{\mathbf{P}}(s) &:= \bigcap_{p \in C^{\mathbf{P}}} CC_{\mathbf{P}}(update_{\mathbf{P}}(p, s))
\end{aligned}
$$

$$
\begin{aligned}
may^{\mathbf{P}}(n) &:= \left| May^{\mathbf{P}}(s) \right|, \text{where } s \in S^{\neq} \subsetneq M^*, |s| = n \\
must^{\mathbf{P}}(n) &:= \left| Must^{\mathbf{P}}(s) \right|, \text{where } s \in S^{\neq} \subsetneq M^*, |s| = n
\end{aligned}
$$

$S^{\neq}$: set of finite access sequences with pairwise different accesses

Definitions of Metrics

$$\text{Evict}^{\mathbf{P}} := \min\left\{n \mid may^{\mathbf{P}}(n) \leq n\right\},$$
$$\text{Fill}^{\mathbf{P}} := \min\left\{n \mid must^{\mathbf{P}}(n) = k\right\},$$

where k is **P**'s associativity.

Relation: Pred. Metrics $\leftrightarrow$ Rel. Competitiveness

Let $P(k)$ be $(1, 0)$-miss-competitive relative to policy $Q(l)$, then

(i) $Evict^P(k) \geq Evict^Q(l)$,

(ii) $mls^P(k) \geq mls^Q(l)$.

Alternative Pred. Metrics $\leftrightarrow$ Rel. Competitiveness

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Let l be the smallest associativity, such that LRU(l) is $(1, 0)$-miss-competitive relative to $P(k)$. Then

$$\text{Alt-Evict}^P(k) = l.$$

Let l be the greatest associativity, such that $P(k)$ is $(1, 0)$-miss-competitive relative to LRU(l). Then

$$\text{Alt-mls}^P(k) = l.$$

Size of Transition System

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$$\underbrace{2^{l+l'}}_{\text{status bits of } \mathbf{P} \text{ and } \mathbf{Q}} \cdot \underbrace{\sum_{i=0}^{k} \binom{k}{i}}_{\text{non-empty lines in } \mathbf{P}} \cdot \underbrace{\sum_{i'=0}^{k'} \binom{k'}{i'}}_{\text{non-empty lines in } \mathbf{Q}} \cdot \underbrace{\sum_{j=0}^{\min\{i,i'\}} \binom{i}{j}\binom{i'}{j} j!}_{\text{number of overlappings in non-empty lines}}$$

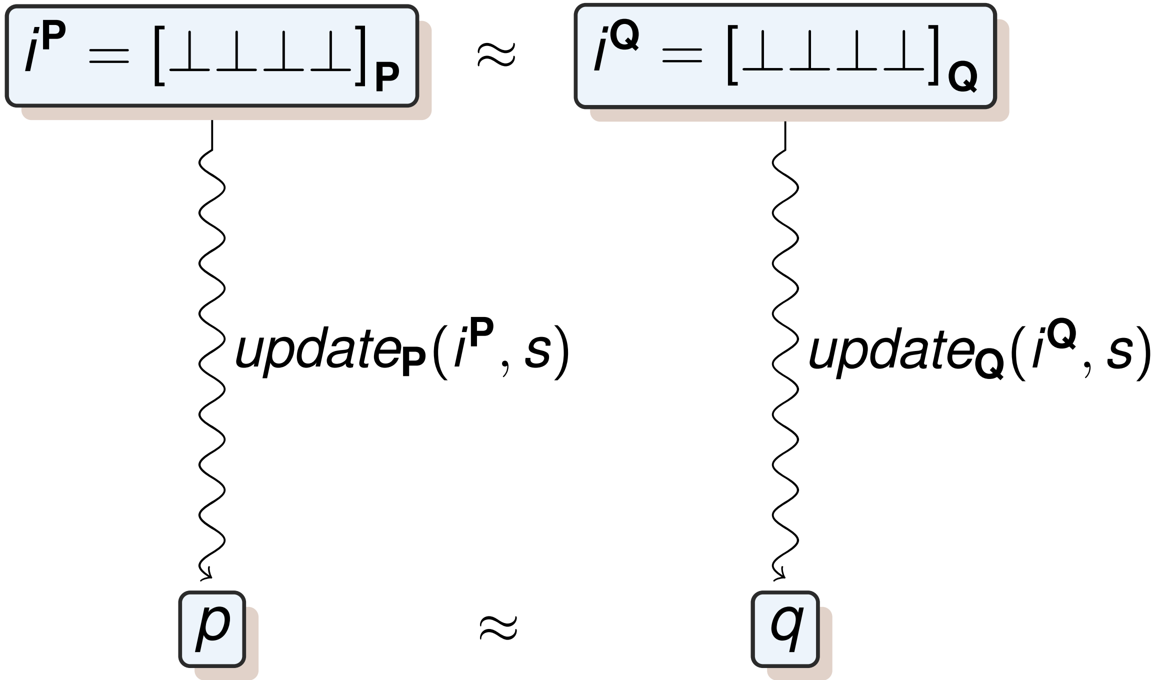
$$\sum_{j=0}^{\min\{k,k'\}} \binom{k}{j}\binom{k'}{j} j! \leq k! \cdot k'! \sum_{j=0}^{\min\{k,k'\}} \frac{1}{(k-j)!j!(k'-j)!}$$

$$\leq k! \cdot k'! \sum_{j=0}^{\infty} \frac{1}{j!} = e \cdot k! \cdot k'!$$

This can be bounded by

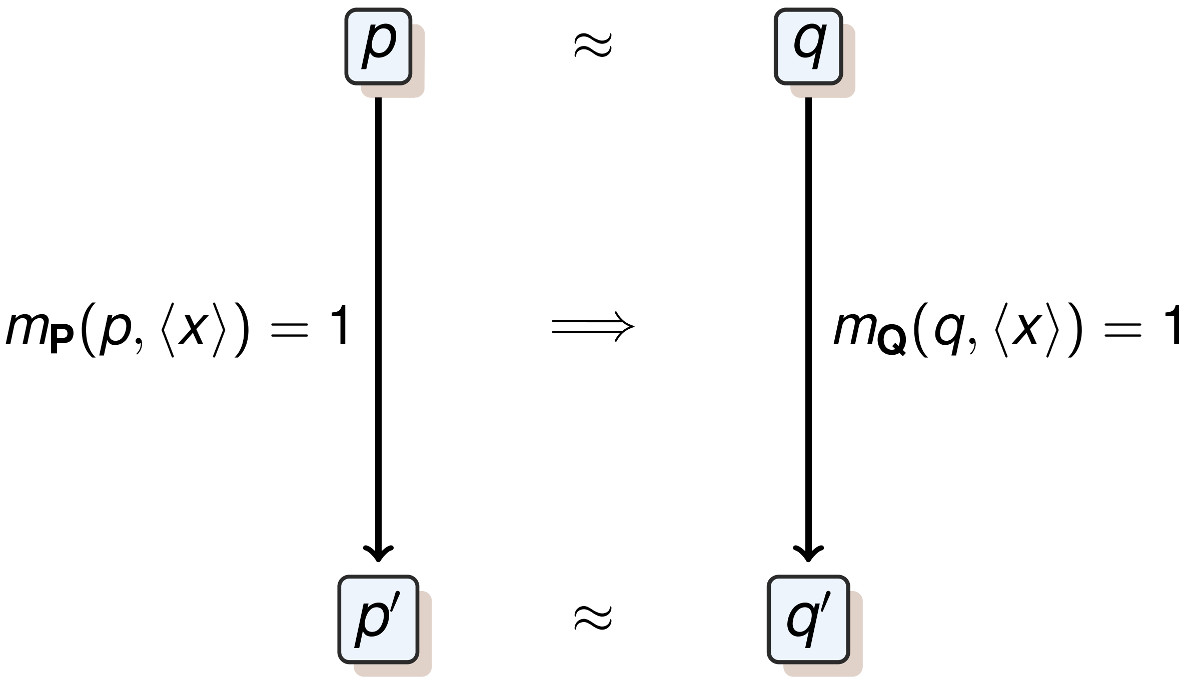
$$2^{l+l'+k+k'} \leq |(C_k^l \times C_{k'}^{l'})/\approx| \leq 2^{l+l'+k+k'} \cdot \underbrace{e \cdot k! \cdot k'!}_{\text{bound on number of overlappings}}$$

Compatible States

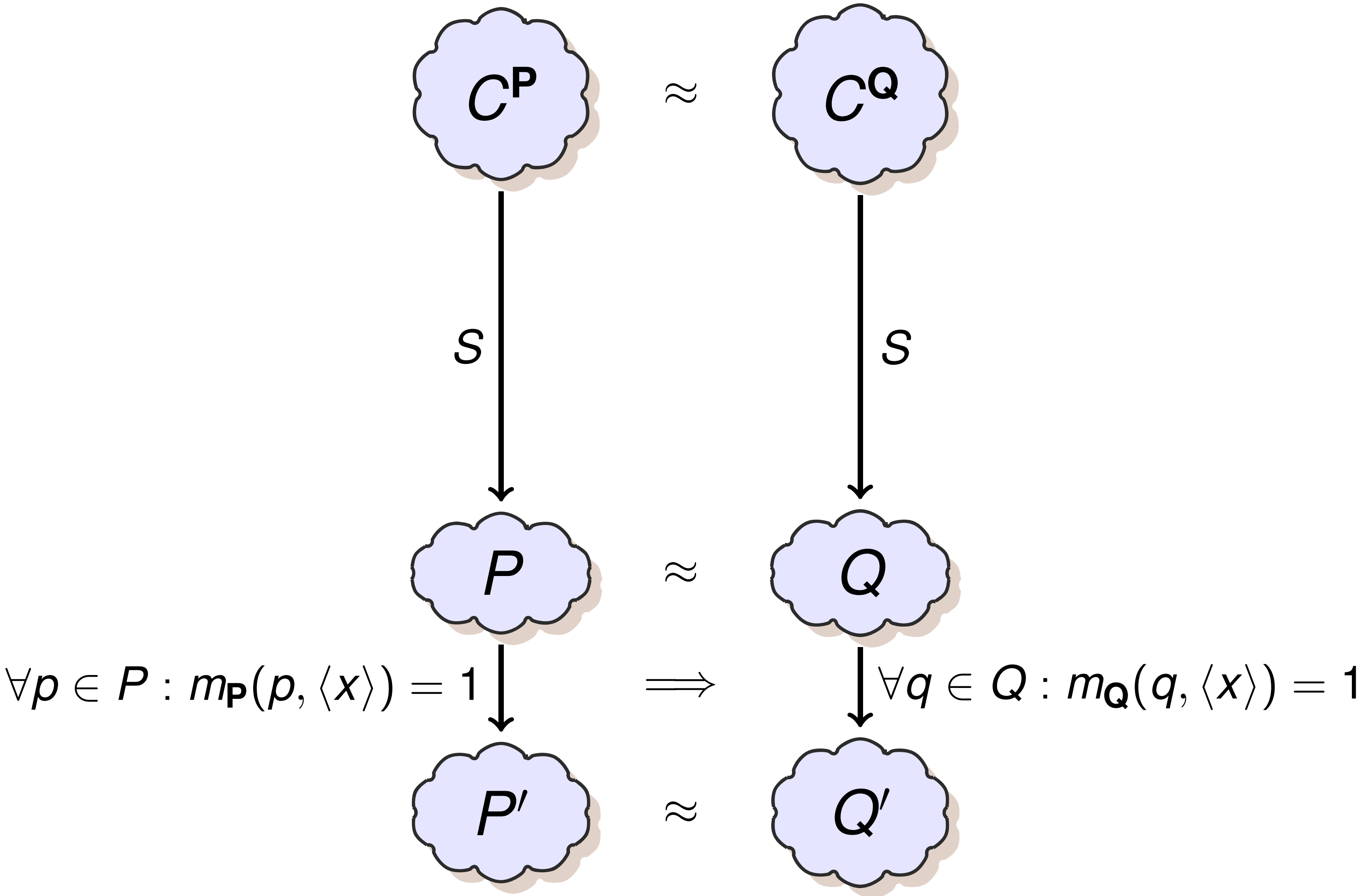


$(1, 0)$-Competitiveness and May/Must-Analyses

Let **P** be $(1, 0)$-competitive relative to **Q**, then



$(1, 0)$-Competitiveness and May/Must-Analyses



Case Study: Impact of Sensitivity

- Simple model of execution time from Hennessy & Patterson (2003)
- CPI_{hit} = Cycles per instruction assuming cache hits only
- $\frac{\text{Memory accesses}}{\text{Instruction}}$ including instruction and data fetches

$$\frac{T_{wc}}{T_{meas}} = \frac{\text{CPI}_{hit} + \frac{\text{Memory accesses}}{\text{Instruction}} \times \text{Miss rate}_{wc} \times \text{Miss penalty}}{\text{CPI}_{hit} + \frac{\text{Memory accesses}}{\text{Instruction}} \times \text{Miss rate}_{meas} \times \text{Miss penalty}}$$

$$= \frac{1.5 + 1.2 \times 0.20 \times 50}{1.5 + 1.2 \times 0.05 \times 50} = \frac{13.5}{4.5} = 3$$